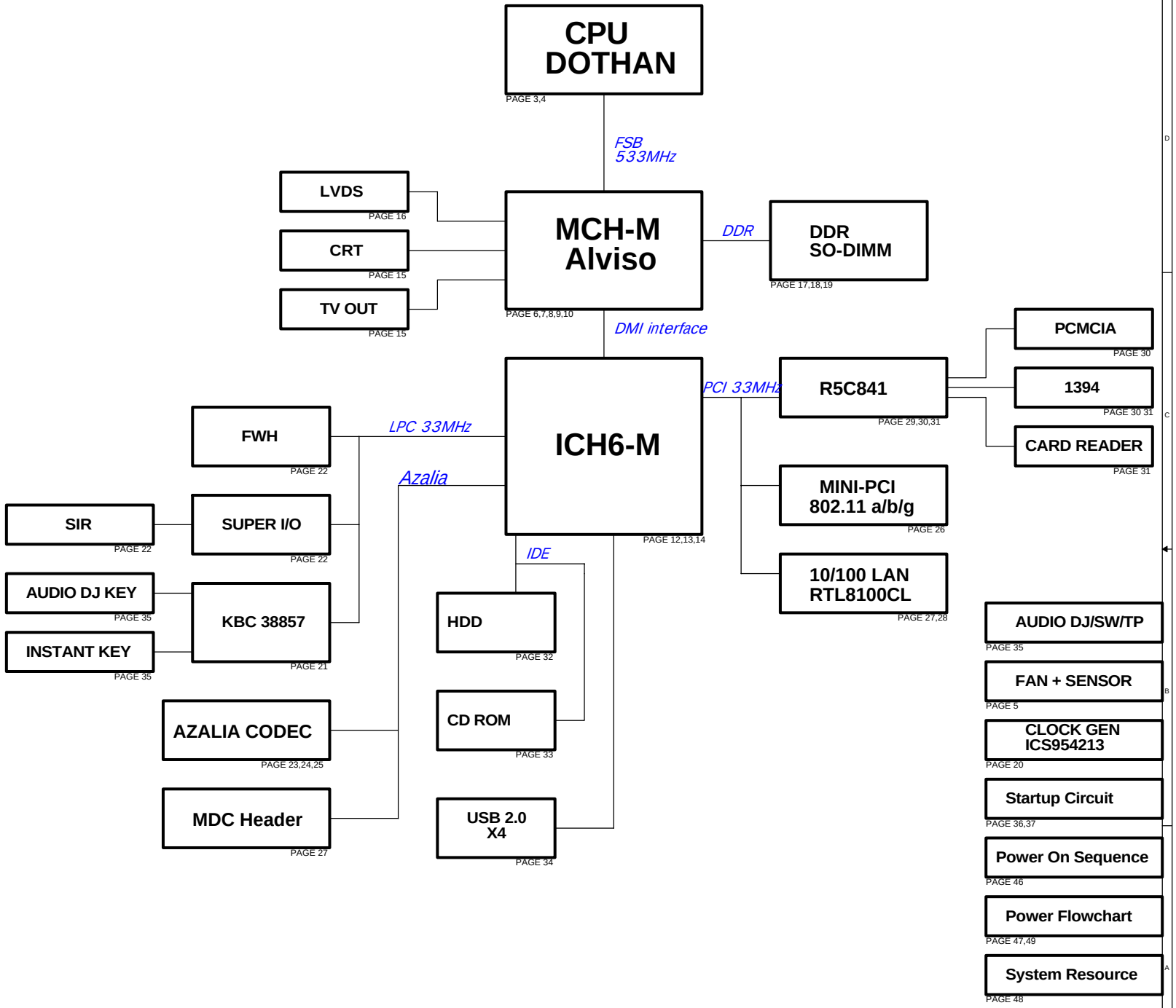
A3A CONTEXT

01_BLOCK DIAGRAM
02_REVISION LIST
03_DOYHAN CPU(1)
04_DOTHAN CPU(2)
05_THERMAL SENSOR,FAN
06_ALVISO GMCH(1)
07_ALVISO PCIE(2)
08_ALVISO DDR SLOT(3)
09_ALVISO POWER(4)
10_ALVISO GND(5)
11_GMCH STRAPPING/LVDS TRANS
12_ICH6M_SATA,LPC,IDE(1)
13_ICH6M_USB,PCI/E,PMIO(2)
14_ICH6M_PWR,GND(3)
15_CRT&TV OUT CONN
16_LVDS&INVERTER(CAMERA,WLAN)
17_DDR_SODIMM
18_DDR_DATA TERMINATION
19_DDR_ADDRESS TERMINATION
20_CLOCK GEN ICS954213
21_KBC M38857
22_FWH,SIO,SIR
23_AZALIA ALC880
24_AMPLIFIER 2 CHANNEL
25_MIC,LINE-IN JACK
26_MINI-PCI
27_LAN_RTL8100CL
28_RJ11/45,MDC,PRN
29_PCI CARDBUS R5C841
30_PCI PCMCIA SOCKET A
31_PCI IEEE1394A,3IN1 CON
32_HDD CONNECTOR
33_Q/SW,CD-ROM CONNECTOR
34_USB CONNECTOR
35_DJ BOARD/SW/TP
36_STARTUP CIRCUIT(1)
37_STARTUP CIRCUIT(2)
38_VCORE
39_SYSTEM(3V,5V)
40_2.5V,1.5V,1.8V,1.05V
41_VCCA,DDR(1.25VS)
42_PIC/BAT CONN/PWOK/THERM PT
43_CHARGE
44_BATLOW/SD#
45_LOAD SWITCH
46_POWER ON SEQUENCE
47_POWER FLOW CHART
48_SYSTEM RESOURCE
49_HISTORY



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 1 of 50	

REVISION LIST

R1.0 2005/01/10

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
~~+1.5VSUS~~	~~1.5V~~	~~270 mA~~
+2.5V	2.5V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	18 mils

37.5 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN2	9.5 mils

50 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN2	5 mils

55 OHM	WIDTH
TOP/BOT	5.5 mils
IN1/IN2	4.5 mils

75 OHM	WIDTH
TOP/BOT	4 mils
IN1/IN3	3.5 mils

Differential

85 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 4 mils
IN1/IN2	4.5 mils/ 4 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 5 mils
IN1/IN2	4.5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	6 mils/ 11 mils
IN1/IN2	5 mils/ 12 mils

110 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 13 mils
IN1/IN2	4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 GND
L3 IN1
L4 IN2
L5 GND
L6 BOT

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```
SIGNAL  IN:   VR_VID[0..5]
              PM_DPRSLPVR
              STP_CPU#
              PM_PSI#
              CPU_VRON
              MCH_OK
        OUT:  DELAY_VR_PWRGD
              CLK_PWR_GD#

POWER   IN:   AC_BAT_SYS
              +5VO
              +3VO
        OUT:  +VCORE
```

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```
SIGNAL  IN:   SUSC#_PWR
              VSUS_ON

POWER   IN:   AC_BAT_SYS

        OUT:  +12VO
              +3VO
              +5VO
```

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```
SIGNAL  IN:   SUSB#_PWR
              SUSC#_PWR
              CPU_VRON

POWER   IN:   AC_BAT_SYS
              +5VO

        OUT:  +1.8V
              +1.5VS
              +2.5VS
              +VCC_GMCH_CORE
              +5VALWAYS
              +3VALWAYS
              +VCCP
```

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```
SIGNAL  IN:   SUSB#_PWR

POWER   IN:   +3V
              +1.8V

        OUT:  +0.9VS
```

ASUSTeK COMPUTER INC	Title : REVISION LIST	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
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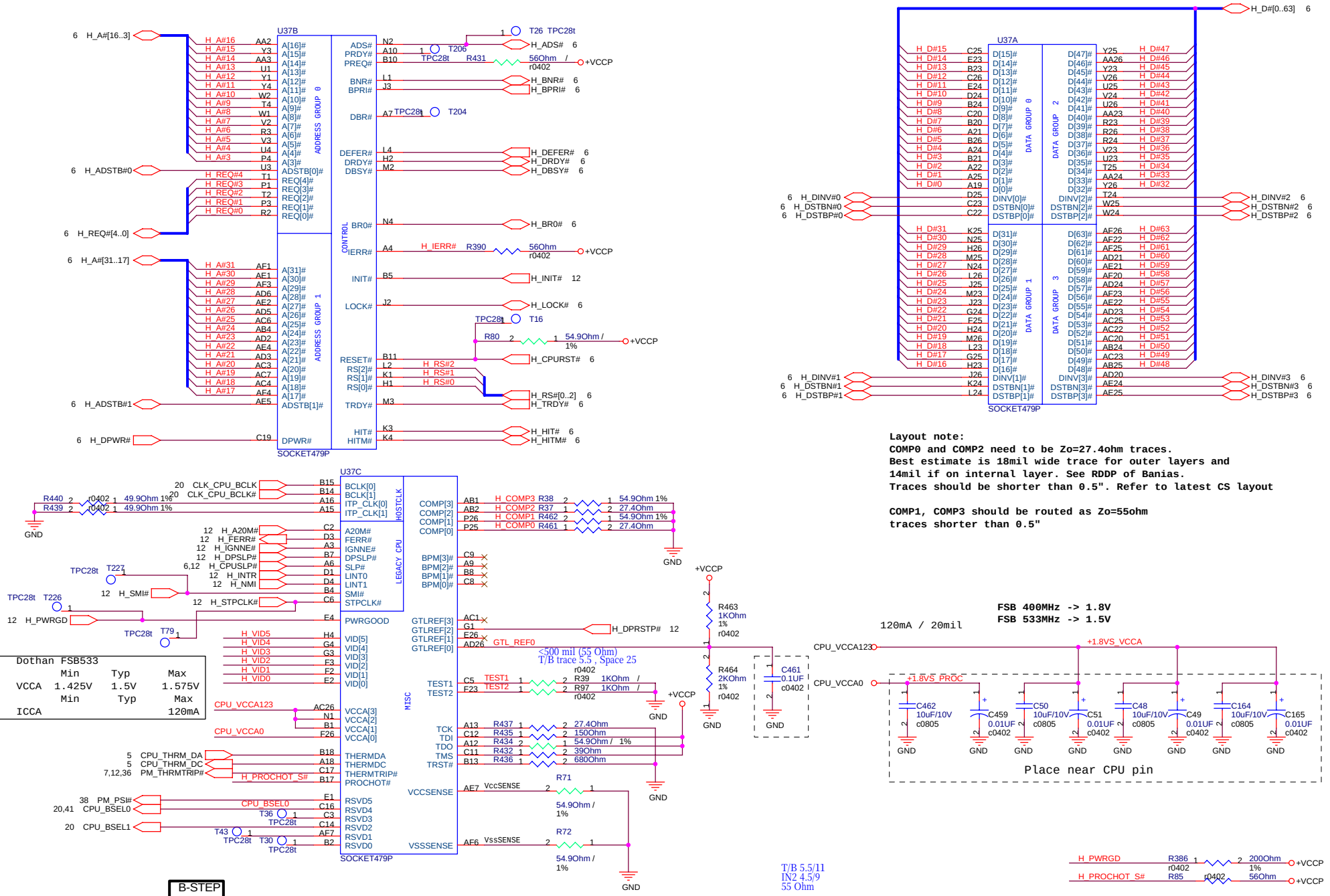


Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"

Dothan FSB533

	Min	Typ	Max
VCCA	1.425V	1.5V	1.575V
	Min	Typ	Max
ICCA			120mA

Bclk	FSB	BSEL1	B-STEP BSEL0
100	400	0	1
133	533	0	0

ASUSTeK COMPUTER INC

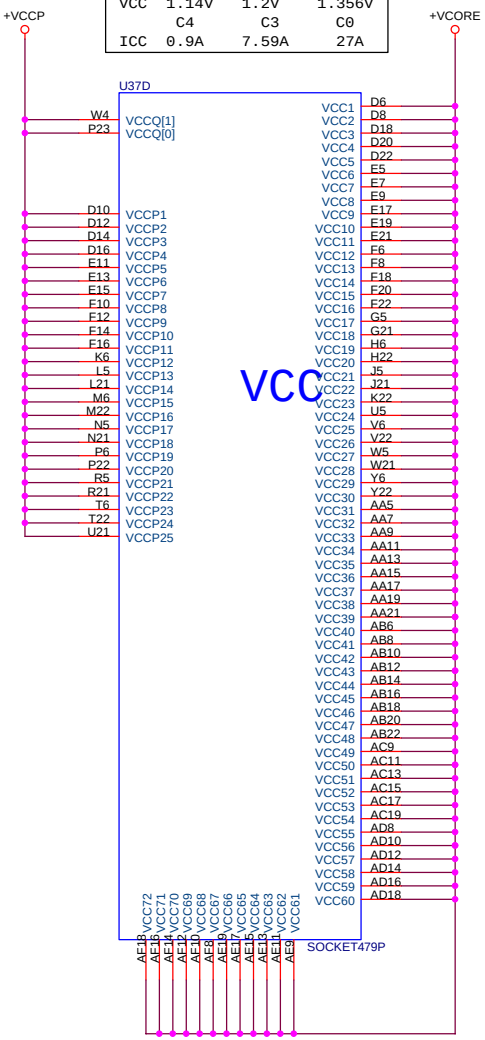
Title : DOTHAN CPU (1)

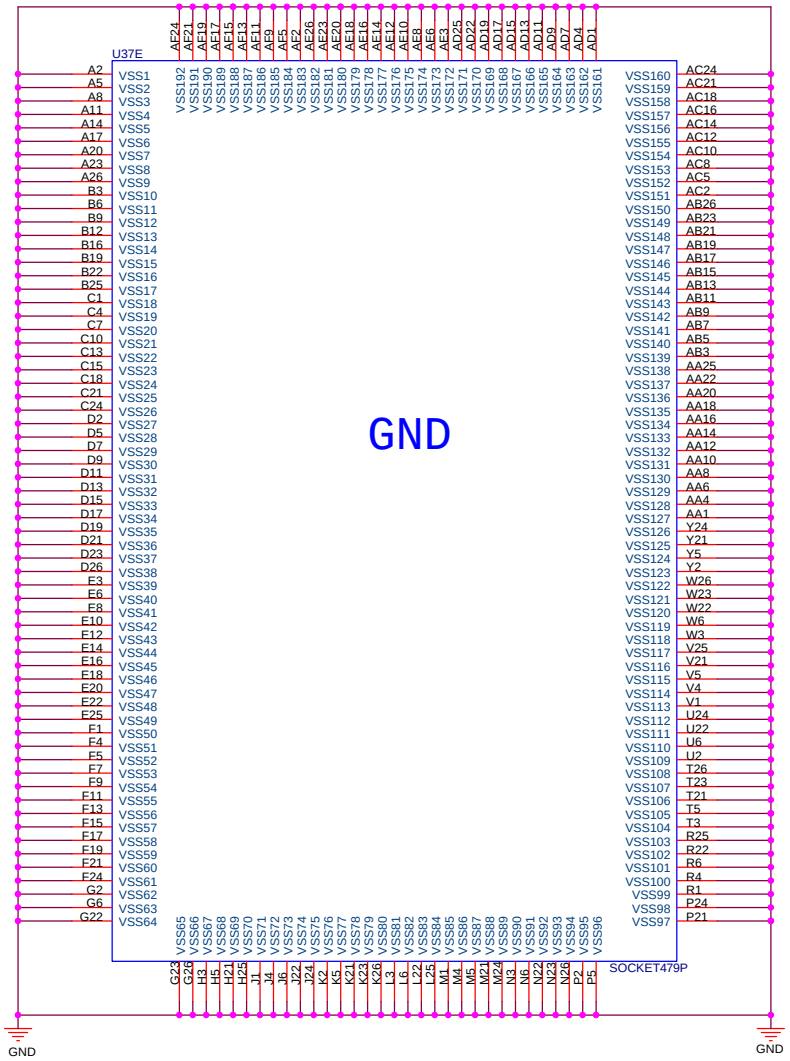
Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 3 of 50

Dothan FSB533	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A



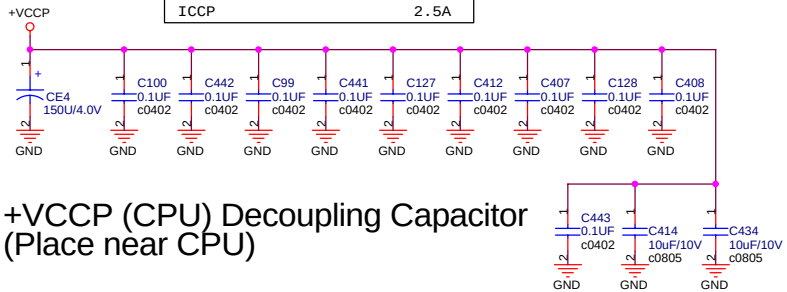


MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

ASUSTeK COMPUTER INC

Title : DOTHAN CPU (2)

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

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Fan Speed Control

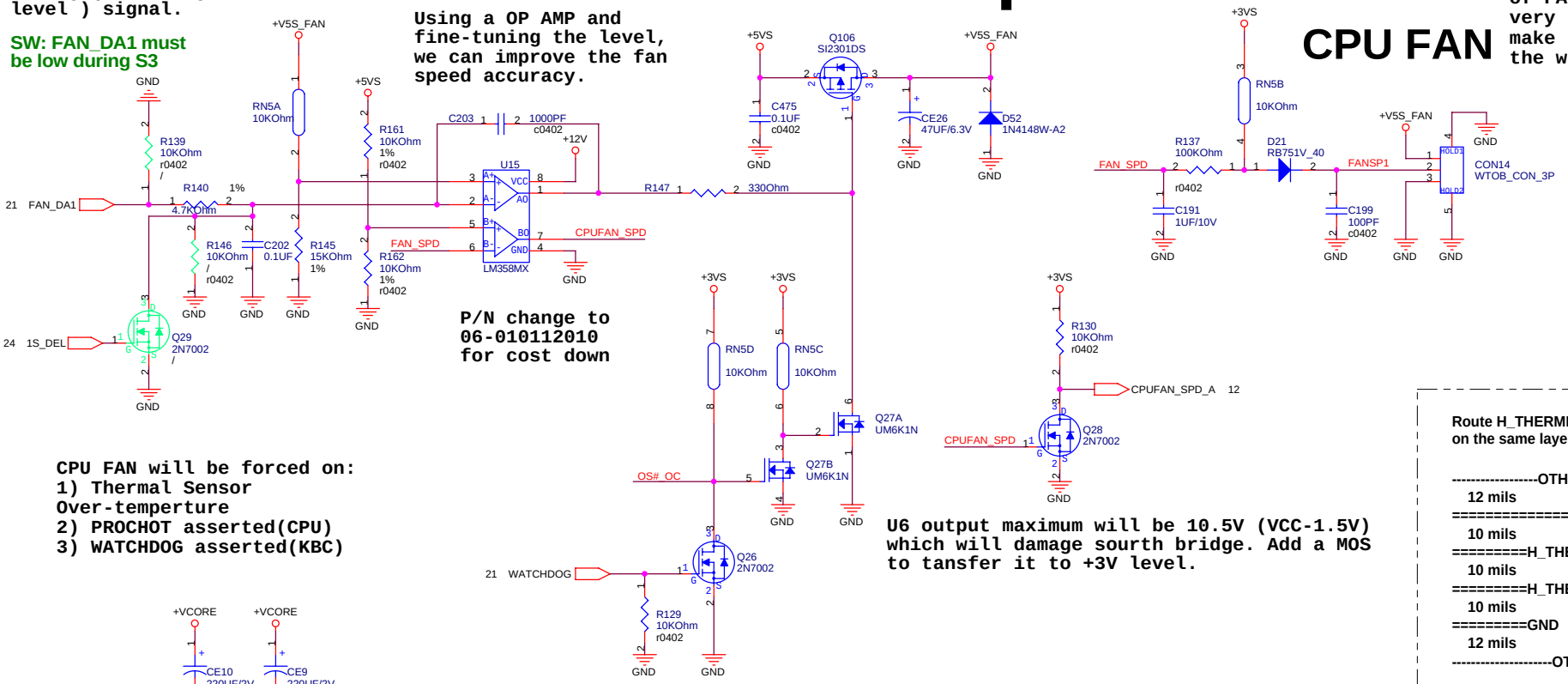
CPU FAN

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



P/N change to 06-010112010 for cost down

CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

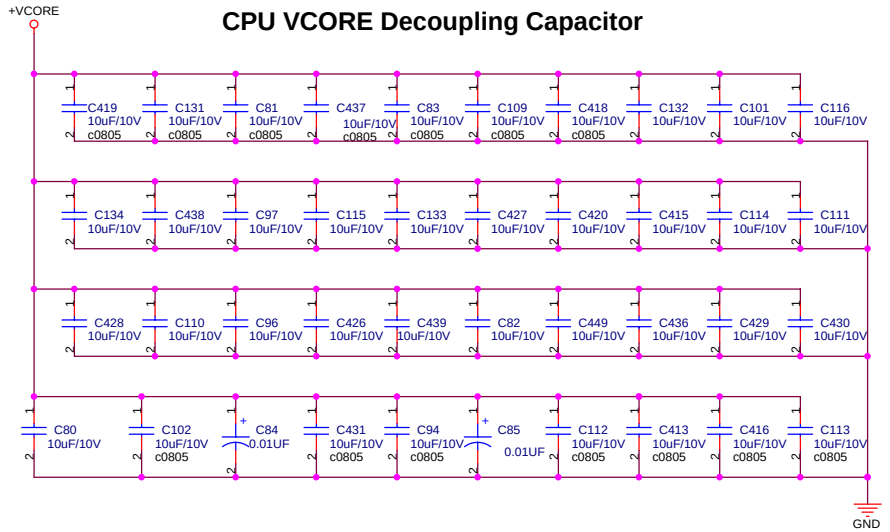
U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

CPU VCORE Decoupling Capacitor

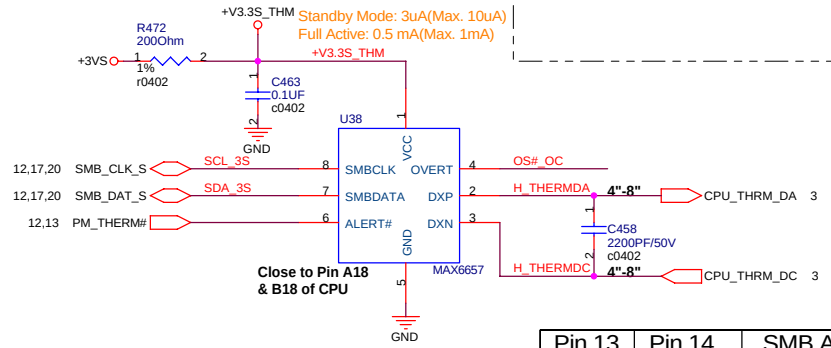


Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

Four 200 uF are located in IMVP4

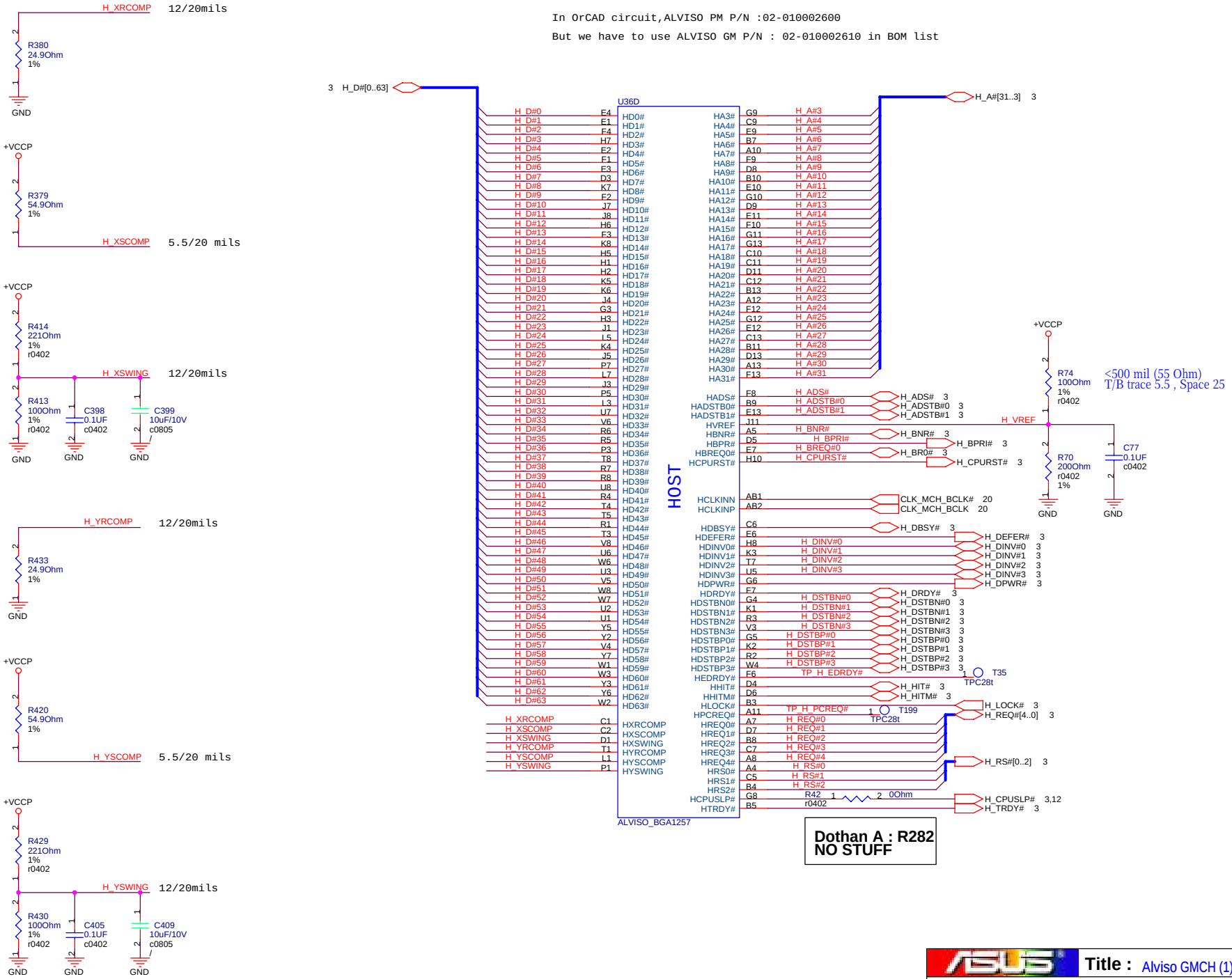


Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

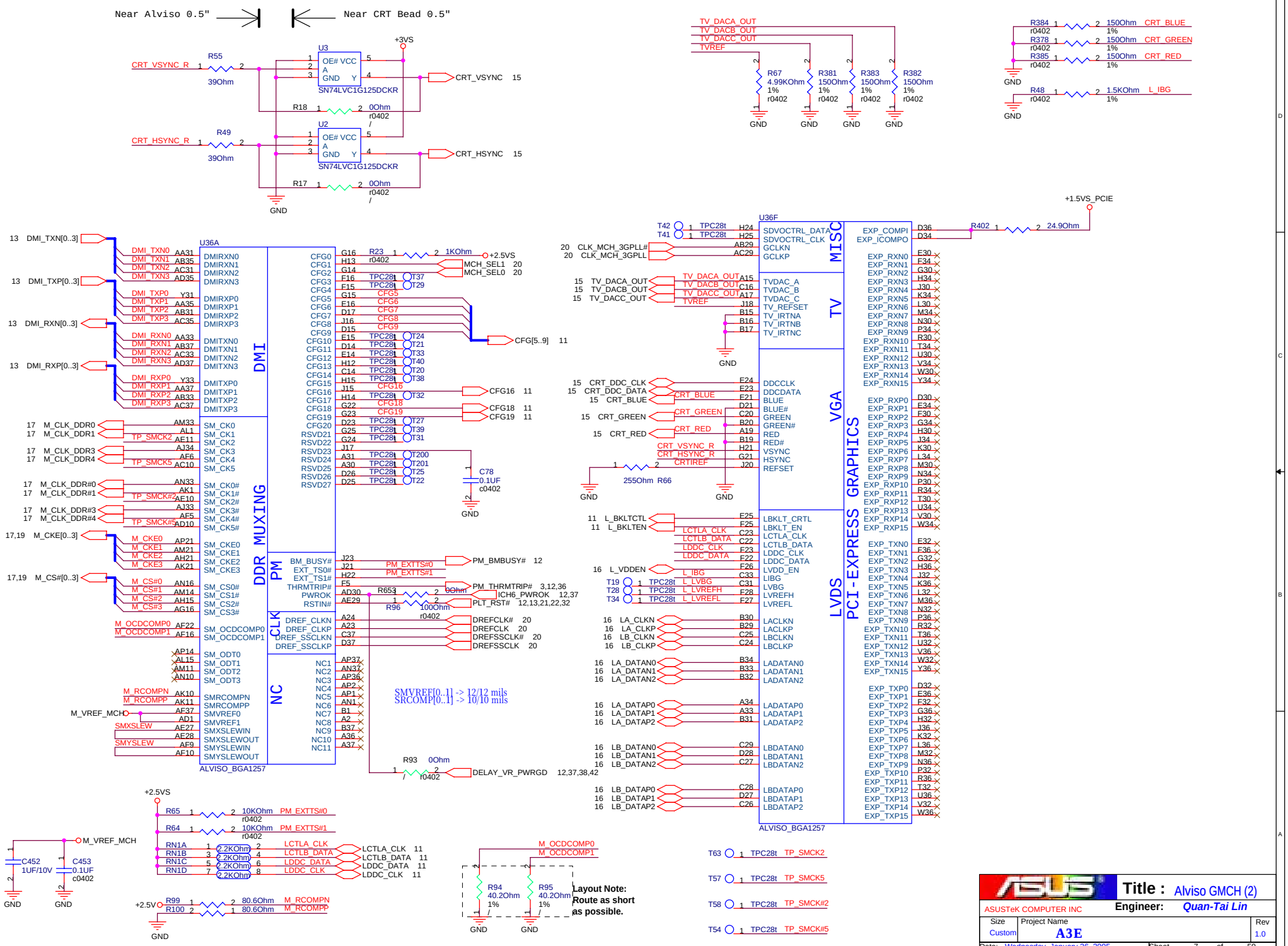
ASUSTeK COMPUTER INC	Title : THER-SENSOR,FAN	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 5 of 50	

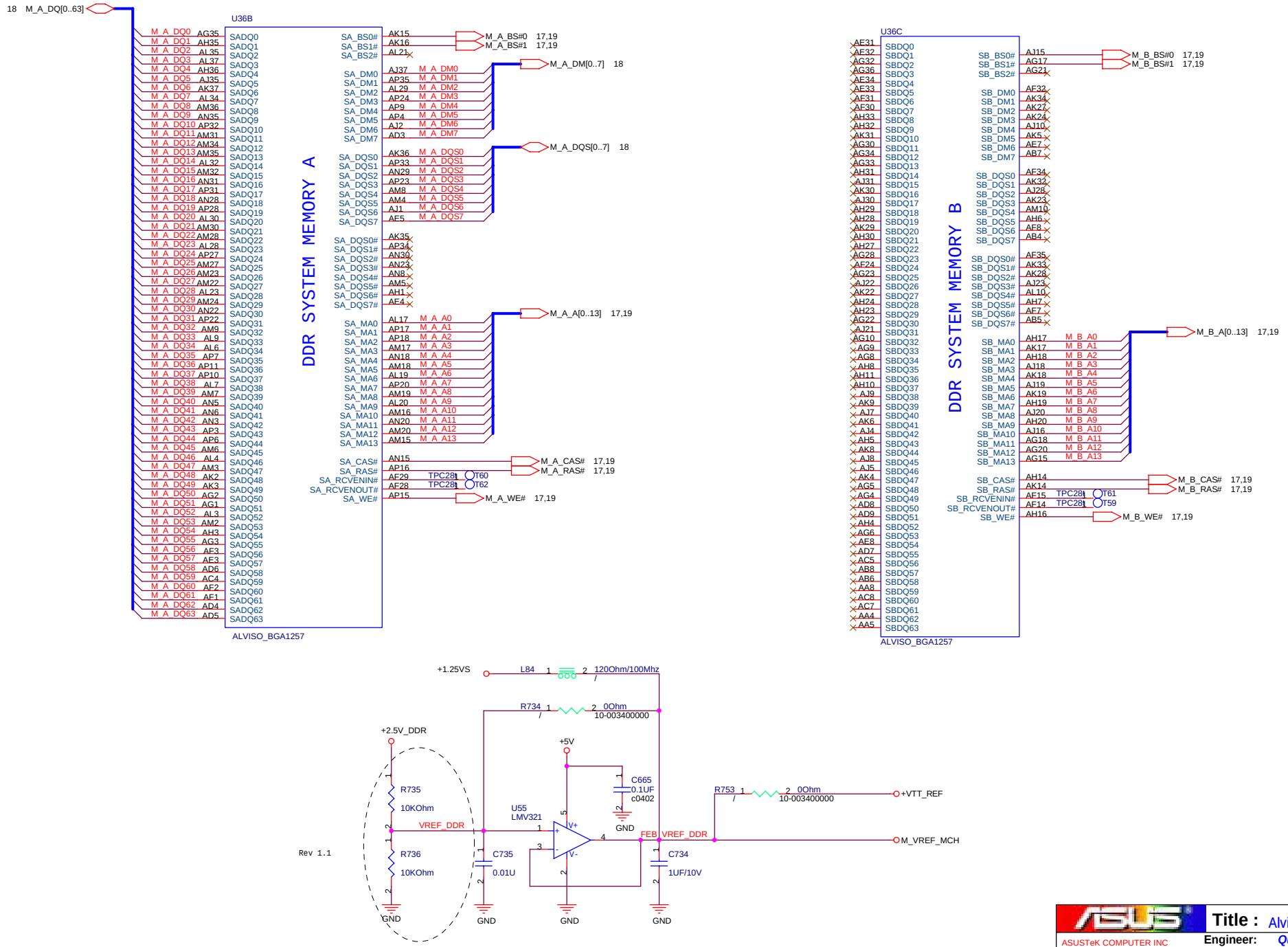
In OrCAD circuit,ALVISO PM P/N :02-010002600

But we have to use ALVISO GM P/N : 02-010002610 in BOM list

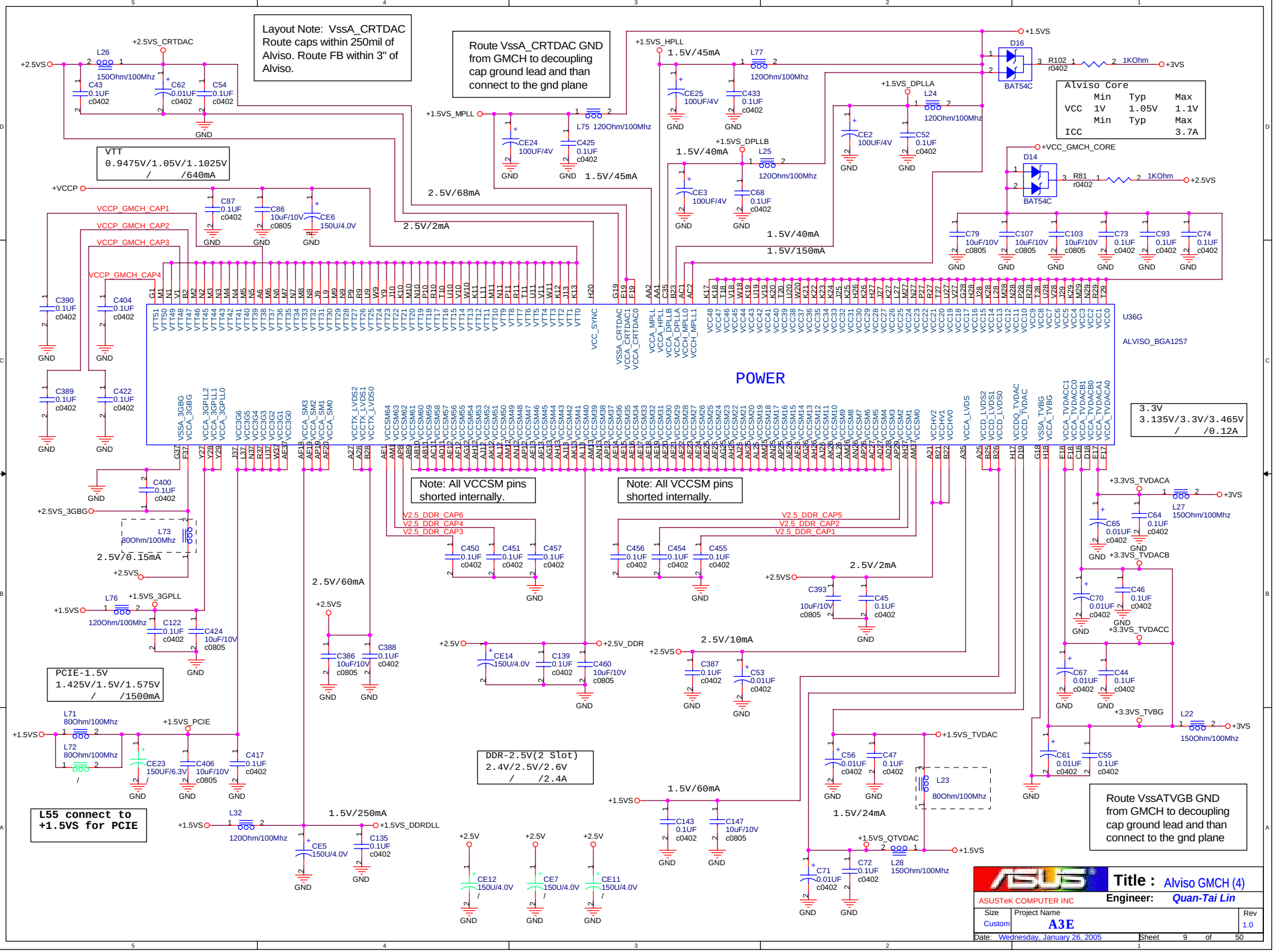


Title :	Alviso GMCH (1)
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E
Rev	1.0
Date: Wednesday, January 26, 2005	Sheet 6 of 50


Near Alviso 0.5"
Near CRT Bead 0.5"
U3
U2
SN74LVC1G125DCKR
CRT_VSYNC_R
CRT_HSYNC_R
R55
R49
39Ohm
R18
R17
0Ohm
r0402
+3VS
CRT_VSYNC 15
CRT_HSYNC 15
GND
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TVREF
R67
4.99KOhm
1%
R381
150Ohm
R383
R382
R384
R378
R385
R48
1.5KOhm
L_IBG
CRT_BLUE
CRT_GREEN
CRT_RED
U36A
U36F
ALVISO_BGA1257
DMI
DDR MUXING
PM
CLK
NC
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
+1.5VS_PCIE
R402
24.9Ohm
+2.5VS
MCH_SEL1 20
MCH_SEL0 20
CFG[5..9] 11
CFG16 11
CFG18 11
CFG19 11
C78
0.1UF
c0402
PM_BMBUSY# 12
PM_THRMTRIP# 3,12,36
ICH6_PWROK 12,37
PLT_RST# 12,13,21,22,32
DREFCLK# 20
DREFCLK 20
DREFSSCLK# 20
DREFSSCLK 20
DELAY_VR_PWRGD 12,37,38,42
SMVREF[0..1] -> 12/12 mils
SRCOMP[0..1] -> 10/10 mils
M_VREF_MCH
C452
1UF/10V
C453
0.1UF
c0402
R65
R64
10KOhm
PM_EXTTS#0
PM_EXTTS#1
RN1A
RN1B
RN1C
RN1D
2.2KOhm
LCTLA_CLK
LCTLB_DATA
LDDC_DATA
LDDC_CLK
R99
R100
80.6Ohm
M_RCOMPN
M_RCOMPP
R94
R95
40.2Ohm
Layout Note:
Route as short
as possible.
TP_SMCK2
TP_SMCK5
TP_SMCK#2
TP_SMCK#5
Title : Alviso GMCH (2)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 7 of 50



ASUSTeK COMPUTER INC	Title : Alviso GMCH (3)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 8 of 50		


Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Alviso Core
Min Typ Max
VCC 1V 1.05V 1.1V
Min Typ Max
ICC 3.7A
VTT
0.9475V/1.05V/1.1025V
/ /640mA
POWER
U36G
ALVISO_BGA1257
3.3V
3.135V/3.3V/3.465V
/ /0.12A
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PCIE-1.5V
1.425V/1.5V/1.575V
/ /1500mA
DDR-2.5V(2 Slot)
2.4V/2.5V/2.6V
/ /2.4A
L55 connect to +1.5VS for PCIE
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Title : Alviso GMCH (4)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
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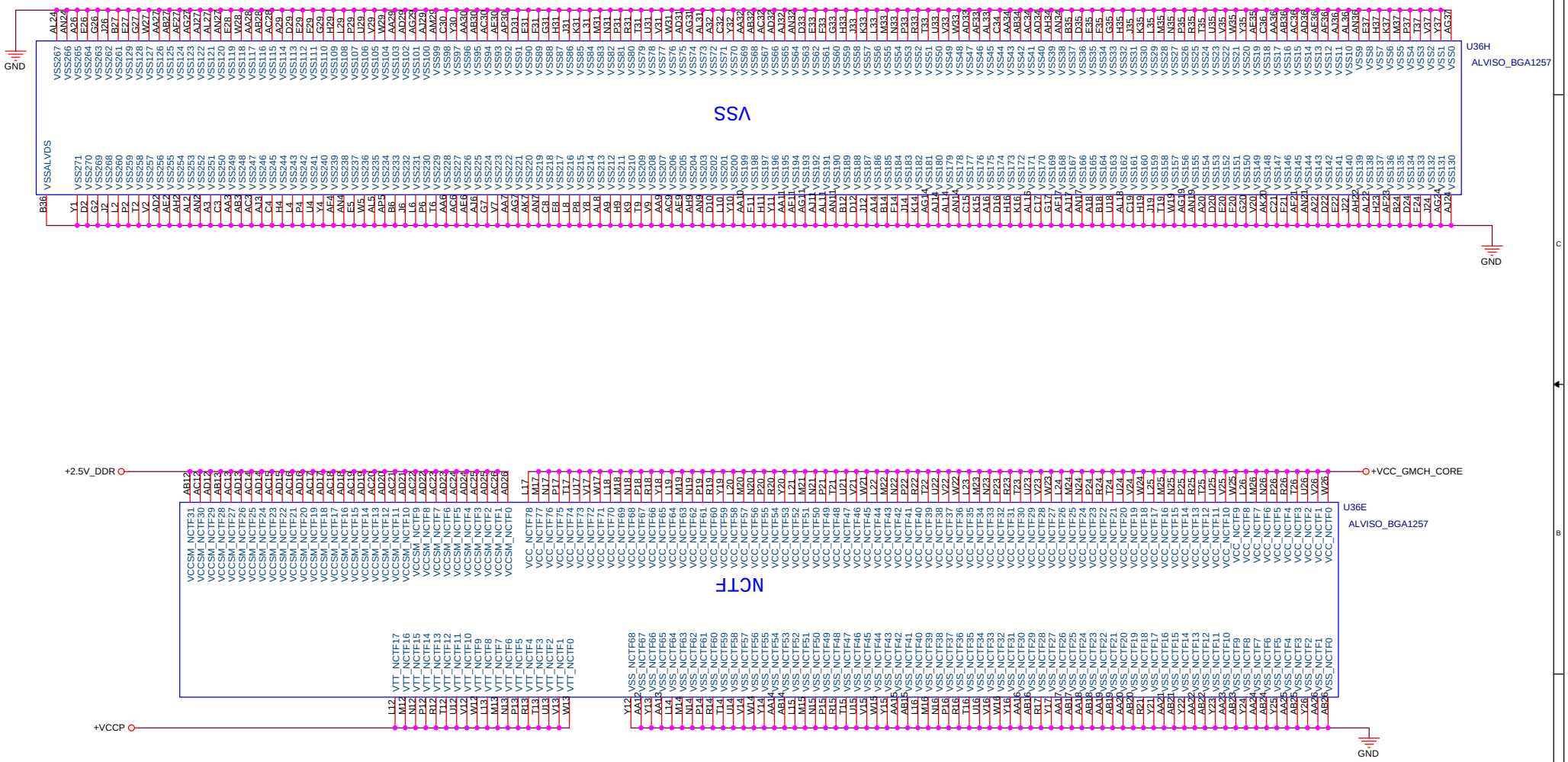
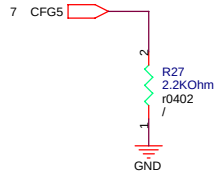


ASUSTeK COMPUTER INC	Title : Alviso GMCH (5)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 10 of 50	

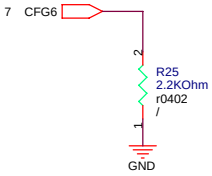
CFG[2:0] are HVCMOS (+2.5VS)
CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
CFG[19..18] have internal pulldown resistors./HVCMOS(+2.5VS)/
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

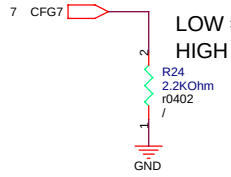
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)

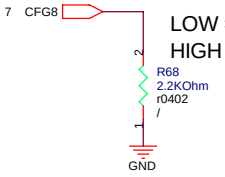


CFG7 : CPU STRAP



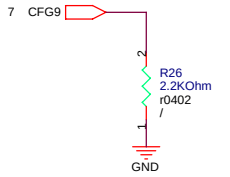
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG8 : PCI-X POWER Saving

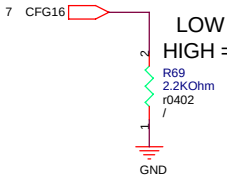


LOW = PCI-X POWER Saving
HIGH (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

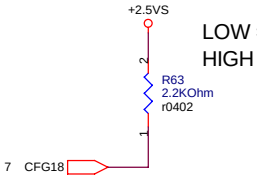


CFG16 : FSB DYNAMIC ODT



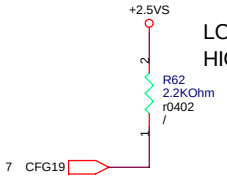
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG18 : VCC SELECT

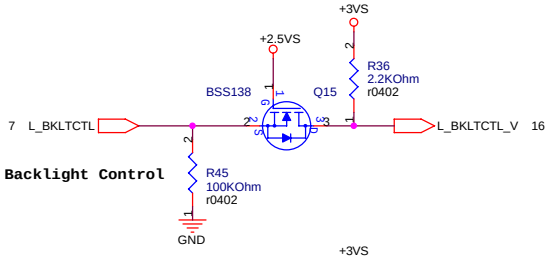


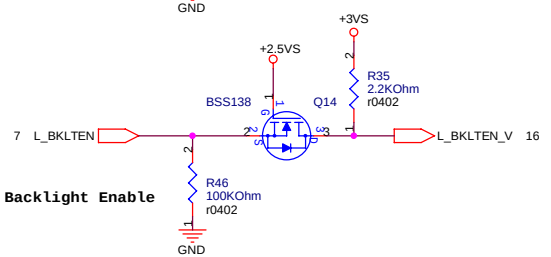
LOW = 1.05V (Default)
HIGH = 1.5V

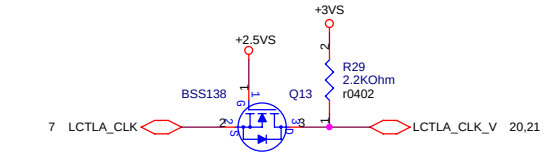
CFG19 : VTT SELECT

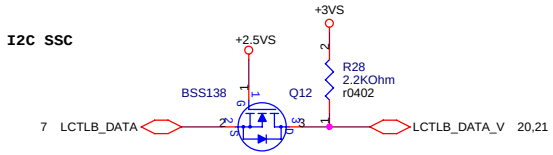


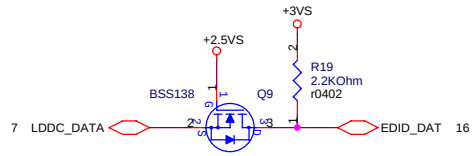
LOW = 1.05V (Default)
HIGH = 1.2V

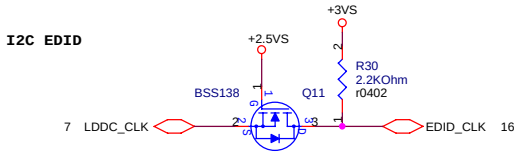












ASUSTeK COMPUTER INC	Title : GMCH Strapping		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 11 of 50		

ICH6-M from 02-010002500 change to 02-010004402
on bom list

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

U20C

32,33 IDE_PDD[0..15]
IDE_PDD15 AD13 DD_15
IDE_PDD14 AG15 DD_14
IDE_PDD13 AE15 DD_13
IDE_PDD12 AC13 DD_12
IDE_PDD11 AB13 DD_11
IDE_PDD10 AB12 DD_10
IDE_PDD9 AF13 DD_9
IDE_PDD8 AE13 DD_8
IDE_PDD7 AB11 DD_7
IDE_PDD6 AD11 DD_6
IDE_PDD5 AC11 DD_5
IDE_PDD4 AE14 DD_4
IDE_PDD3 AD12 DD_3
IDE_PDD2 AF14 DD_2
IDE_PDD1 AE15 DD_1
IDE_PDD0 AD14 DD_0

SATA_0RXN AE3 — R538 1 2 0Ohm r0402
SATA_0RXP AD3
SATA_0TXN AG2 — TPC28t T110
SATA_0TXP AF2 — TPC28t T111
SATA_1RXN AC5 — R532 1 2 0Ohm r0402
SATA_1RXP AD5
SATA_1TXN AF4 — TPC28t T105
SATA_1TXP AG4 — TPC28t T106
SATA_2RXN AD7 — R529 1 2 0Ohm r0402
SATA_2RXP AC7
SATA_2TXN AF6 — TPC28t T104
SATA_2TXP AG6 — TPC28t T103
SATA_3RXN AC9 — R526 1 2 0Ohm r0402
SATA_3RXP AD9
SATA_3TXN AF8 — TPC28t T101
SATA_3TXP AG8 — TPC28t T102
GND

SATA_CLKN AC2
SATA_CLKP AC1

32,33 IDE_PDDACK# AB15 DDACK#
32,33 IDE_PDDREQ AB14 DDREQ
32,33 IDE_PDIOR# AE16 DIOR#
32,33 IDE_PDIOW# AC14 DIOW#
32,33 IDE_PIORDY AF16 IORDY
+3VS — R246 4.7KOhm r0402

SATARBIAS# AG11
SATARBIAS AF11
PLACE WITHIN 500mils of ICH6 ball
R256 0Ohm r0402 — GND
R288 0Ohm r0402 — GND

32,33 IDE_PDA0 AC16 DA0
32,33 IDE_PDA1 AB17 DA1
32,33 IDE_PDA2 AC17 DA2

32,33 IDE_PDCS1# AD16 DCS1#
32,33 IDE_PDCS3# AE17 DCS3#

R243 8.2KOhm r0402 — +3VS
32,33 INT_IRQ14 AB16 IDEIRQ

SMBCLK Y4 — SMB_CLK
SMBDATA W5 — SMB_DAT
R281 1 2 2.2KOhm — +3VSUS
R282 1 2 2.2KOhm — +3VS
SMB_CLK_S — R275 1 2 2.2KOhm
SMB_DAT_S — R278 1 2 2.2KOhm

LINKALERT# Y5 — LINKALERT# 13
SMLINK_0 W4 — SM_LINK0 13
SMLINK_1 U6 — SM_LINK1 13

SATALED# AC19 — TPC28t T233
SATA_0GP/GPI26 AF17 — SATA_DET_#0 13 3 H_FERR#
SATA_1GP/GPI29 AE18 — PCB_ID2 13
SATA_2GP/GPI30 AE18 — PCB_ID0 13
SATA_3GP/GPI31 AG18 — PCB_ID1 13
INTRUDER# AA3 — R541 1M r0402 — +VCC_RTC

RSMRST# Y3 — PM_RSMRST# 36

RTCX1 Y1 — RTC_X1 — C308 2 1 12PF/50V c0402
RTCX2 Y2 — RTC_X2 — R303 10MOhm
X3 SIDE 32.768KHZ +/-20ppm/12.5PF
RTCRST# AA2 — RTC_RST# — C313 2 1 12PF/50V c0402 — GND
INTVRMEN AA5 — 33KOhm R543 — +VCC_RTC
SPKR F8 — SB_SPKR 23

INTERNAL PULL-DOWN
PULL-UP : NO REBOOT

ICH6_M

JRST1 1 2 — GND
Rev 1.1
R544 2 1 180KOhm — +VCC_RTC
C537 0.1UF c0402 — GND

+5VS
5,17,20 SMB_CLK_S — Q64 2N7002 — SMB_CLK
+5VS
5,17,20 SMB_DAT_S — Q72 2N7002 — SMB_DAT

U20D

+3VSUS — R300 8.2KOhm r0402 — CB_SD#
R701 8.2KOhm r0402 — +3VS — P4 LDRQ_1#/GPIO41

21,22,26 LPC_AD0 — P2 LAD_0/FWH0
21,22,26 LPC_AD1 — N3 LAD_1/FWH1
21,22,26 LPC_AD2 — N5 LAD_2/FWH2
21,22,26 LPC_AD3 — N4 LAD_3/FWH3
13,22 LPC_DRQ#0 — N6 LDRQ_0#
21,22,26 LPC_FRAME# — P3 LFRAME#/FWH4

23,28 ACZ_BCLK — R268 1 2 33Ohm — C10 ACZ_BIT_CLK
23,24,28 ACZ_RST# — R262 1 2 0Ohm — A10 ACZ_RST#
23 ACZ_SDIN0 — F11 ACZ_SDIN_0
28 ACZ_SDIN1 — F10 ACZ_SDIN_1
ACZ_SDIN_2
23,28 ACZ_SDOUT — R273 1 2 47Ohm 1% — T99 1 TPC28t — B10 ACZ_SDOUT
+3VS — R270 2 r0402 1 1KOhm — C9 ACZ_SYNC
23,28 ACZ_SYNC — R271 1 2 33Ohm — B9 CLK14
20 CLK_ICH14 — E10

T237 1 TPC28t — D12 EE_CS
F13 EE_DIN
D11 EE_DOUT
B12 EE_SHCLK
INTERNAL PULL-UP
PULL-DOWN : RESERVED
R523 1KOhm r0402 — GND

F12 LAN_CLK
B11 LAN_RSTSYNC
E12 LAN_RXD_0
E11 LAN_RXD_1
C13 LAN_RXD_2
C12 LAN_TXD_0
C11 LAN_TXD_1
E13 LAN_TXD_2

H_CPUSLP# R193 : B STEP NO STUFF
H_DPRSTP# R231 : A STEP NO STUFF

21 A20GATE — AF22 A20GATE
3 H_A20M# — AF23 A20M#
3,6 H_CPUSLP# — R193 1 r0402 2 0Ohm — AF27 CPUSLP#
13,38 PM_DPRSLPVR — AE20 DPRSLPVR/TP_1
3 H_DPRSTP# — R192 1 r0402 2 0Ohm — AE24 DPRSLP#/TP_2
3 H_DPSLP# — AD27 DPSTP#
3 H_IGNNE# — AG26 IGNNE#
22 FWH_INIT# — AE22 INIT3_3V#
+VCCP — 56Ohm R197 r0402 — 3 H_INIT# — AE27 INIT#
3 H_INTR — AG24 INTR
R196 r0402 56Ohm — AF24 FERR#
3 H_NMI — AF25 NMI
21 RCIN# — AD23 RCIN#
13,21,22,26,29 INT_SERIRQ — AB20 SERIRQ
3 H_SMI# — AG27 SMI#
3 H_STPCLK# — AE26 STPCLK#
3,7,36 PM_THRMTRIP# — R194 r0402 56Ohm — AE23 THRMTRIP#
R190 75Ohm r0402 — +VCCP

BMBUSY#/GPI6 AD19 — R226 8.2KOhm r0402 — +3VS
GPI7 AE19 — R227 1 r0402 2 8.2KOhm — PM_BMBUSY# 7
GPI8 R1 — EXTSMI# 21
SMBALERT#/GPIO11 W6 — R542 1 r0402 2 10KOhm — +3VSUS
GPI12 M2 — KB_SCI# 13,21
GPI13 R6 — SIO_SMI# 13,22
STP_PCI#/GPO18 AC21 — STP_PCI# 13,20
GPIO19 AB21 — PWRLED_1HZ 13
STP_CPU#/GPO20 AD22 — STP_CPU# 13,20,38
GPIO21 AD20 — T308 1
GPIO23 AD21 — TPC28t — FWH_WP# 22
GPIO24 V3 — 802_LED_EN# 13,35
GPIO25 P5 — CB_SD# — CB_SD# 29
GPIO27 R3 — OP_SD# 24
GPIO28 T3 — TPC28t T241
CLKRUN#/GPIO32 AE19 — PM_CLKRUN# 13,21,26,27,29
GPIO33 AF20 — CPUFAN_SPD_A 5
GPIO34 AC18 — WLAN_ON# 16,26
CPUPWRGD/GPIO49 AG25 — H_PWRGD — H_PWRGD 3

MCH_SYNC# AG21 — MCH_SYNC# 13
PWRBTN# U1 — PM_PWRBTN# 36
RI# T2 — RING# — RING# 13

SLP_S3# T4 — R549 1 r0402 2 100Ohm
SLP_S4# T5 — R536 1 r0402 2 100Ohm — SUSB# 16,22,27,29,35,37,42,45
SLP_S5# T6 — TPC28t T236 — SUSC# 34,35,36,45

SUS_STAT#/LPCPD# W3 — SUS_STAT# 13
TPC28t T238
SUSCLK V6 — SUSCLK
SYS_RESET# U2 — R297 1 r0402 2 10KOhm — R293 1 r0402 2 0Ohm — ICH6_PWROK — +3VSUS
LAN_RST# V5 — LAN_RST#
BATLOW# V2 — PM_BATLOW# 13
TP_3 U3 — R296 2 1 10KOhm r0402 — GND
TP_3 INTERNAL PULL-UP
PULL-DOWN : PCI
Express Port chain test

R307 2 0Ohm r0402 — DELAY_VR_PWRGD 7,37,38,42
VRMPWRGD AF21 — R295 1 2 0Ohm r0402 — ICH6_PWROK 1 T66 TPC28t
THRM# AC20 — PM_THERM# 5,13
LAN_RST# R548 1 0Ohm r0402
R547 10KOhm r0402 — PLT_RST# 7,13,21,22,32 — GND

WAKE# U5 — R534 1 r0402 2 1KOhm — +3VSUS
PWROK AA1 — ICH6_PWROK — ICH6_PWROK 7,37
R306 10KOhm r0402 — GND

ICH6_M

DELAY 18~25ms
+RTCBAT — BAT1 BATT_HOLDER_2P — GND
+3VA — R545 1 r0402 2 1KOhm 1 — D56 2 — RB715F — +VCC_RTC
C543 1UF/10V — GND
PM_BATLOW# — D36 2 1 1N4148W-A2 — BAT_LLOW#_OC 21,42

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2"
from the series resistor

ASUSTeK COMPUTER INC	Title : ICH6_M (1)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 12 of 50	

PLT_RST#
ICH6,Alviso/KBC/FWH/HDD

U20A

26,27,29 PCI_PAR — E1 PAR
26,27,29 PCI_DEVSEL# — C3 DEVSEL#
20 CLK_ICHPCI — G6 PCICLK
26,27,29 PCI_RST# — R2 PCIRST#
7,12,21,22,32 PLT_RST# — R5 PLTRST#
26,27,29 PCI_IRDY# — A3 IRDY#
22,26,27,29 PCI_PME# — P6 PME#
26,27,29 PCI_SERR# — G5 SERR#
26,27,29 PCI_STOP# — J1 STOP#
PCI_LOCK# — C5 PLOCK#
26,27,29 PCI_TRDY# — J2 TRDY#
26,27,29 PCI_PERR# — E3 PERR#
26,27,29 PCI_FRAME# — J3 FRAME#

T120 1 TPC28t — C1 GNT_0#
29 PCI_GNT#1 — B6 GNT_1#
27 PCI_GNT#2 — F1 GNT_2#
26 PCI_GNT#3 — C8 GNT_3#
T240 1 TPC28t — E7 GNT_4#/GPIO48
GPIO17 — F6 GNT_5#/GPIO17
GPIO16 — D8 GNT_6#/GPIO16

PCI_REQ#0 — L5 REQ_0#
29 PCI_REQ#1 — B5 REQ_1#
27 PCI_REQ#2 — M5 REQ_2#
26 PCI_REQ#3 — B8 REQ_3#
F7 REQ_4#/GPIO40
TPC28t T239 1 — PCI_REQ#5 — E8 REQ_5#/GPIO1
PCI_REQ#6 — B7 REQ_6#/GPIO0

PCI_INTA# — N2 PIRQA#
29 PCI_INTB# — L2 PIRQB#
29 PCI_INTC# — M1 PIRQC#
29 PCI_INTD# — L3 PIRQD#
27 PCI_INTE# — D9 PIRQE#/GPIO2
PCI_INTF# — C7 PIRQF#/GPIO3
26 PCI_INTG# — C6 PIRQG#/GPIO4
26 PCI_INTH# — M3 PIRQH#/GPIO5

CLK_ICHPCI
C516 10PF / c0402
GND

ICH6_M

PCI_AD[0..31] 26,27,29

AD_0 — E2 PCI_AD0
AD_1 — E5 PCI_AD1
AD_2 — C2 PCI_AD2
AD_3 — E5 PCI_AD3
AD_4 — F3 PCI_AD4
AD_5 — E9 PCI_AD5
AD_6 — E2 PCI_AD6
AD_7 — D6 PCI_AD7
AD_8 — E6 PCI_AD8
AD_9 — D3 PCI_AD9
AD_10 — A2 PCI_AD10
AD_11 — D2 PCI_AD11
AD_12 — D5 PCI_AD12
AD_13 — H3 PCI_AD13
AD_14 — B4 PCI_AD14
AD_15 — J5 PCI_AD15
AD_16 — K2 PCI_AD16
AD_17 — K5 PCI_AD17
AD_18 — D4 PCI_AD18
AD_19 — L6 PCI_AD19
AD_20 — G3 PCI_AD20
AD_21 — H4 PCI_AD21
AD_22 — H2 PCI_AD22
AD_23 — H5 PCI_AD23
AD_24 — B3 PCI_AD24
AD_25 — M6 PCI_AD25
AD_26 — B2 PCI_AD26
AD_27 — K6 PCI_AD27
AD_28 — K3 PCI_AD28
AD_29 — A5 PCI_AD29
AD_30 — L1 PCI_AD30
AD_31 — K4 PCI_AD31

C_BE_3# — G2 PCI_C/BE#3 26,27,29
C_BE_2# — G4 PCI_C/BE#2 26,27,29
C_BE_1# — H6 PCI_C/BE#1 26,27,29
C_BE_0# — J6 PCI_C/BE#0 26,27,29

U20B

7 DMI_RXN0 — T25 DMI_0RXN
7 DMI_RXP0 — T24 DMI_0RXP
7 DMI_TXN0 — R27 DMI_0TXN
7 DMI_TXP0 — R26 DMI_0TXP
7 DMI_RXN1 — V25 DMI_1RXN
7 DMI_RXP1 — V24 DMI_1RXP
7 DMI_TXN1 — U27 DMI_1TXN
7 DMI_TXP1 — U26 DMI_1TXP
7 DMI_RXN2 — Y25 DMI_2RXN
7 DMI_RXP2 — Y24 DMI_2RXP
7 DMI_TXN2 — W27 DMI_2TXN
7 DMI_TXP2 — W26 DMI_2TXP
7 DMI_RXN3 — AB24 DMI_3RXN
7 DMI_RXP3 — AB23 DMI_3RXP
7 DMI_TXN3 — AA27 DMI_3TXN
7 DMI_TXP3 — AA26 DMI_3TXP

USBP_0N — C21 — USB_PN0_B — USB_PN0_B 34
USBP_0P — D21 — USB_PP0_B — USB_PP0_B 34
USBP_1N — A20 — USB_PN1_B — USB_PN1_B 34
USBP_1P — B20 — USB_PP1_B — USB_PP1_B 34
USBP_2N — D19 — USB_PN2_B — USB_PN2_B 34
USBP_2P — C19 — USB_PP2_B — USB_PP2_B 34
USBP_3N — A18 — USB_PN3_B — USB_PN3_B 34
USBP_3P — B18 — USB_PP3_B — USB_PP3_B 34
USBP_4N — E17 — USB_PN4_B — USB_PN4_B 16
USBP_4P — D17 — USB_PP4_B — USB_PP4_B 16
USBP_5N — B16 — USB_PN5_B — USB_PN5_B 16
USBP_5P — A16 — USB_PP5_B — USB_PP5_B 16
USBP_6N — C15 — USB_PN6_B — USB_PN6_B 29
USBP_6P — D15 — USB_PP6_B — USB_PP6_B 29
USBP_7N — A14 — TPC28t T95
USBP_7P — B14 — TPC28t T96

+3VSUS
OC_4# — R219 1 — 2 8.2KOhm r0402
OC_5# — R211 1 — 2 8.2KOhm r0402

(USB 4 for CAMERA)
(USB 5 for WLAN)

OC_0# — C27 — USB_OC_01# 34
OC_1# — B27
OC_2# — B26 — USB_OC_23# 34
OC_3# — C26
OC_4#/GPIO9 — C23 — OC_4#
OC_5#/GPIO10 — D23 — OC_5#
OC_6#/GPIO14 — C25 — GPIO14
OC_7#/GPIO15 — C24 — GPIO15

+3VSUS
RN13A 1 — 2 8.2KOhm
RN13B 3 — 4 8.2KOhm
RN13C 5 — 6 8.2KOhm
RN13D 7 — 8 8.2KOhm

T84 1 TPC28t — H25 HSIN_0
T80 1 TPC28t — H24 HSIP_0
G27 HSON_0
G26 HSOP_0
K25 HSIN_1
T81 1 TPC28t — K24 HSIP_1
T85 1 TPC28t — J27 HSON_1
J26 HSOP_1
M25 HSIN_2
T82 1 TPC28t — M24 HSIP_2
T86 1 TPC28t — L27 HSON_2
L26 HSOP_2
P24 HSIN_3
T83 1 TPC28t — P23 HSIP_3
T87 1 TPC28t — N27 HSON_3
N26 HSOP_3

GND

USBRBIAS — B22 — USBRBIAS — R228 1 — 2 22.6Ohm 1% — GND
USBRBIAS# — A22

PLACE within 500 mils of ICH.

+1.5VS — R514 1 — 2 24.9Ohm 1% — F24 DMI_ZCOMP
F23 DMI_IRCOMP

PLACE within 500 mils of ICH.
5.5mil/8mil

CLK48 — A27 — CLK_USB48 20
C271 10PF / c0402 — GND

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK , AC_RST# , AC_SDIN[2:0] ,
AC_SDOUT , AC_SYNC , DPSLPVR ,
LAN_CLK , PDD[7] , SDD[7] ,
PDDREQ , SDDREQ , SPKR ,
USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
EE_DIN , EE_DOUT ,
GNT[B:A]# , GNT[5]# ,
GPIO[17:16] , LAD[3:0]# ,
LDRQ[1:0] , LAN_RXD[2:0] ,
PME# , PWRBTN#

20 CLK_PCIE_ICH# — AD25 DMI_CLKN
20 CLK_PCIE_ICH — AC25 DMI_CLKP

ICH6_M

+3VS

PCI_FRAME# — RP4A 1 — 8.2KOhm 5 10
PCI_IRDY# — RP4B 2 — 8.2KOhm 5 10
PCI_TRDY# — RP4C 3 — 8.2KOhm 5 10
PCI_STOP# — RP4D 4 — 8.2KOhm 5 10
PCI_SERR# — RP4E 6 — 8.2KOhm 5 10
PCI_DEVSEL# — RP4F 7 — 8.2KOhm 5 10
PCI_PERR# — RP4G 8 — 8.2KOhm 5 10
PCI_LOCK# — RP4H 9 — 8.2KOhm 5 10

PCI_INTA# — RP2A 1 — 8.2KOhm 5 10
PCI_INTB# — RP2B 2 — 8.2KOhm 5 10
PCI_INTC# — RP2C 3 — 8.2KOhm 5 10
PCI_INTD# — RP2D 4 — 8.2KOhm 5 10
PCI_INTE# — RP2E 6 — 8.2KOhm 5 10
PCI_INTF# — RP2F 7 — 8.2KOhm 5 10
PCI_INTG# — RP2G 8 — 8.2KOhm 5 10
PCI_INTH# — RP2H 9 — 8.2KOhm 5 10

PCI_REQ#0 — RP3A 1 — 8.2KOhm 5 10
PCI_REQ#1 — RP3B 2 — 8.2KOhm 5 10
PCI_REQ#2 — RP3C 3 — 8.2KOhm 5 10
PCI_REQ#3 — RP3D 4 — 8.2KOhm 5 10
RP3E 6 — 8.2KOhm 5 10
RP3F 7 — 8.2KOhm 5 10
PCI_REQ#5 — RP3G 8 — 8.2KOhm 5 10
PCI_REQ#6 — RP3H 9 — 8.2KOhm 5 10

12,22 LPC_DRQ#0 — RN17A 1 — 8.2KOhm 2
RN17B 3 — 8.2KOhm 4
12 PWRLED_1HZ — RN17C 5 — 8.2KOhm 6
12,21,26,27,29 PM_CLKRUN# — RN17D 7 — 8.2KOhm 8
12 SATA_DET_#0 — R242 1 — r0402 — 2 8.2KOhm

12,38 PM_DPRSLPVR — R230 1 — 2 100KOhm 10-004401040 r0402 — GND

R540 1 — 2 1KOhm r0402 — GPIO17
GND
INTERNAL PULL-UP
PULL-DOWN : Boot BIOS destination select

R525 1 — 2 1KOhm r0402 — GPIO16
GND
INTERNAL PULL-UP
PULL-DOWN :TOP-BLOCK SWAP

PCB_VID 0 1 2
MB V1.0 0 0 0

PCB_VID3 : PROJECT CODE

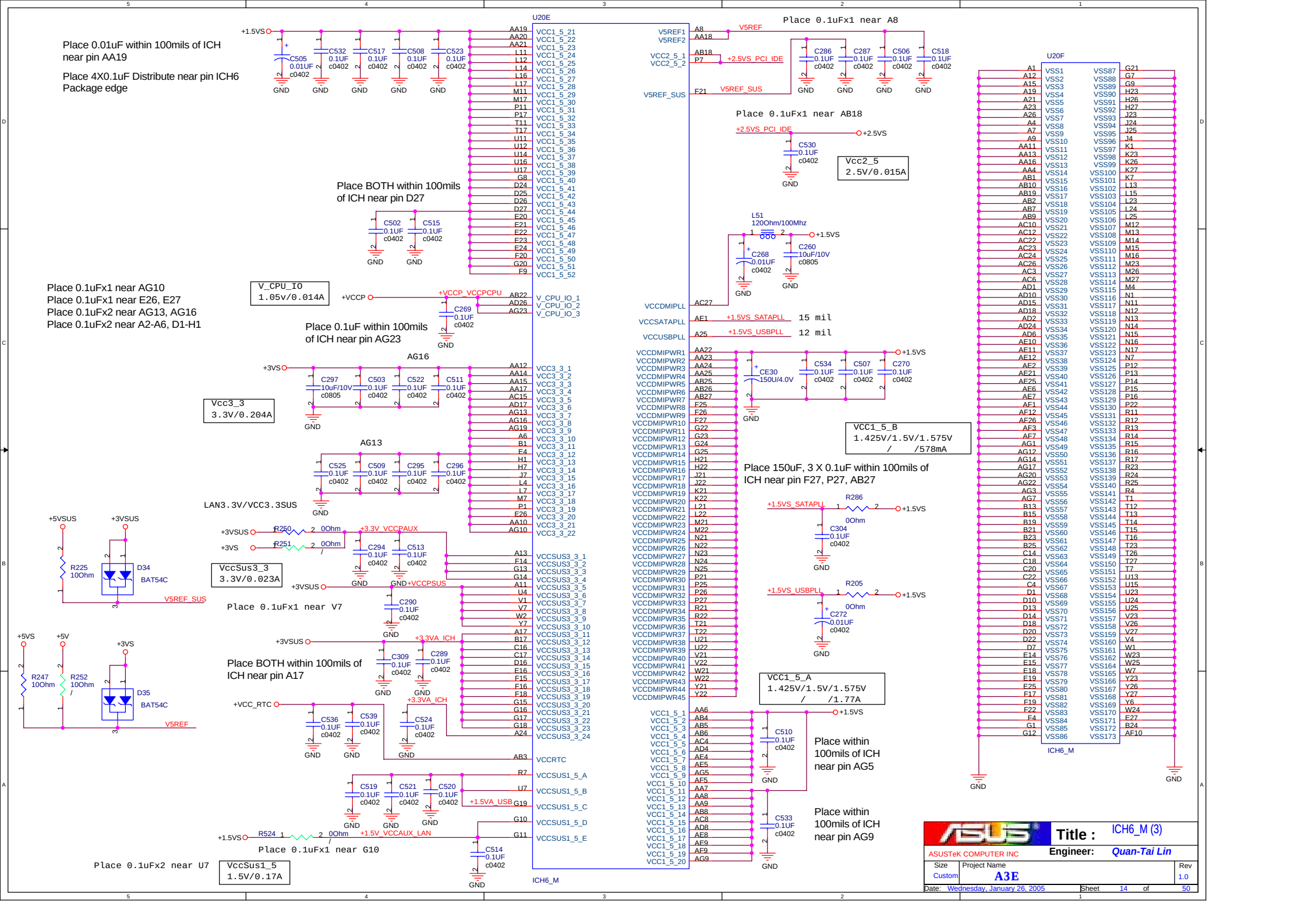
+3VS
R232 8.2KOhm r0402 /
R238 8.2KOhm / r0402
R234 8.2KOhm / r0402
12 PCB_ID0
12 PCB_ID1
12 PCB_ID2
R231 8.2KOhm r0402
R237 8.2KOhm r0402
R233 8.2KOhm r0402
GND

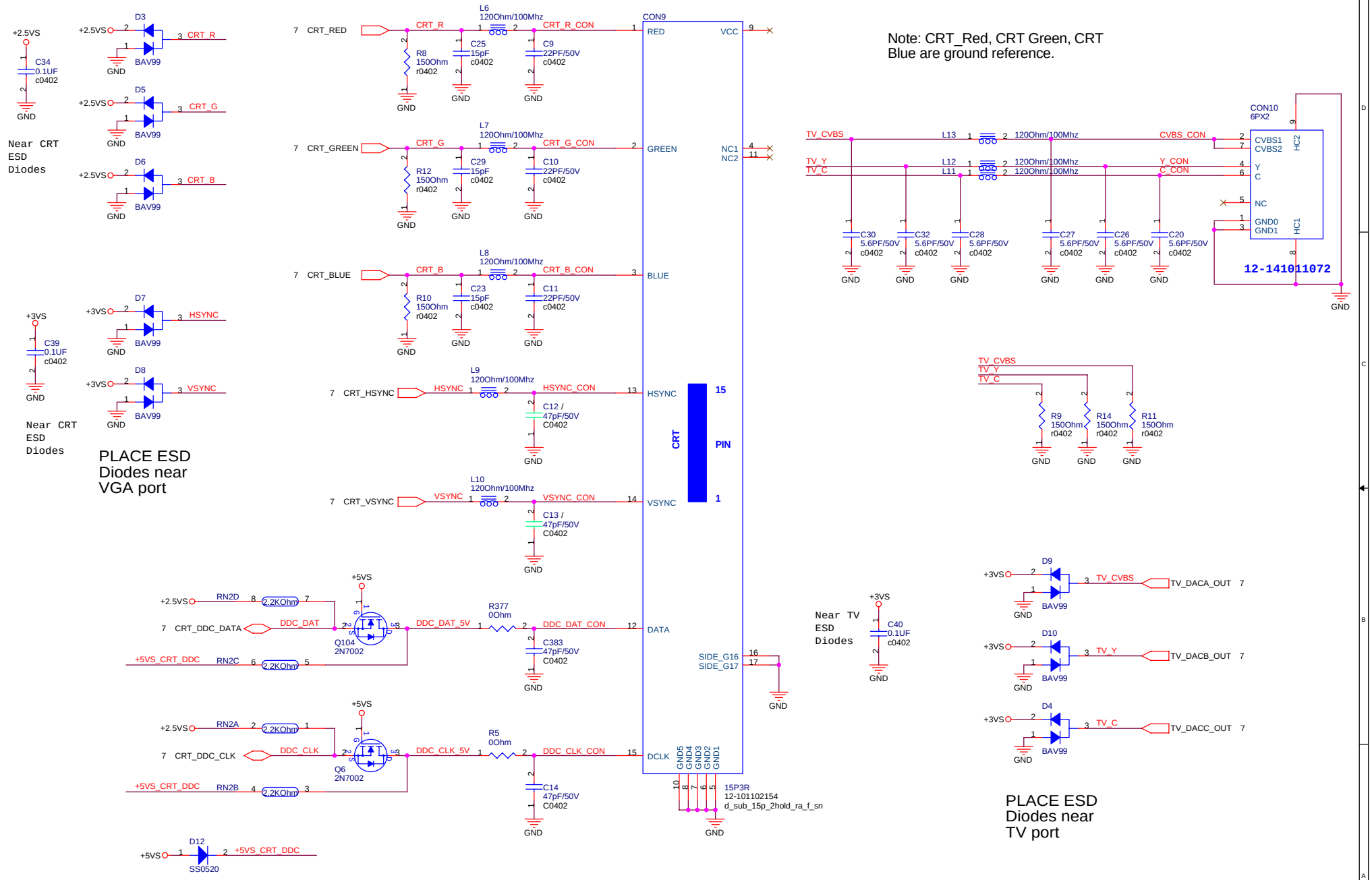
+3VSUS
12 SM_LINK0 — R537 1 — 2 10KOhm r0402
12 LINKALERT# — R531 1 — 2 10KOhm r0402
12 RING# — RN30A 1 — 8.2KOhm 2
12,22 SIO_SMI# — RN30C 3 — 8.2KOhm 4
12 PM_BATLOW# — RN30D 5 — 8.2KOhm 6
7 — 8.2KOhm 8
12 SM_LINK1 — R528 1 — 2 10KOhm r0402
PCI_PME# — R535 1 — 2 10KOhm r0402
12,35 802_LED_EN# — R294 1 — 2 8.2KOhm r0402

+3VS
12,21,22,26,29 INT_SERIRQ — R204 1 — 2 8.2KOhm r0402
12,20 STP_PCI# — R203 1 — 2 10KOhm r0402
12,20,38 STP_CPU# — R216 1 — 2 10KOhm r0402
12 MCH_SYNC# — R215 1 — 2 10KOhm r0402
12 SUS_STAT# — R539 1 — 2 4.7KOhm r0402
5,12 PM_THERM# — R208 1 — 2 8.2KOhm r0402

R298 1 — 2 10KOhm r0402 — +3VSUS
12,21 KB_SCI# — R299 1 — 2 10KOhm r0402 — +3VS

ASUSTeK COMPUTER INC	Title : ICH6_M (2)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 13 of 50		


U20E
Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1
V_CPU_IO
1.05v/0.014A
Place 0.1uF within 100mils of ICH near pin AG23
AG16
Vcc3_3
3.3V/0.204A
AG13
LAN3.3V/VCC3.3SUS
VccSus3_3
3.3V/0.023A
Place 0.1uFx1 near V7
Place BOTH within 100mils of ICH near pin A17
Place 0.1uFx1 near G10
Place 0.1uFx2 near U7
VccSus1_5
1.5V/0.17A
ICH6_M
Place 0.1uFx1 near A8
Place 0.1uFx1 near AB18
Vcc2_5
2.5V/0.015A
15 mil
12 mil
VCC1_5_B
1.425V/1.5V/1.575V
/ /578mA
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
VCC1_5_A
1.425V/1.5V/1.575V
/ /1.77A
Place within 100mils of ICH near pin AG5
Place within 100mils of ICH near pin AG9
U20F
ICH6_M
Title : ICH6_M (3)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 14 of 50



Title : CRT & TV OUT

ASUSTeK COMPUTER INC

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

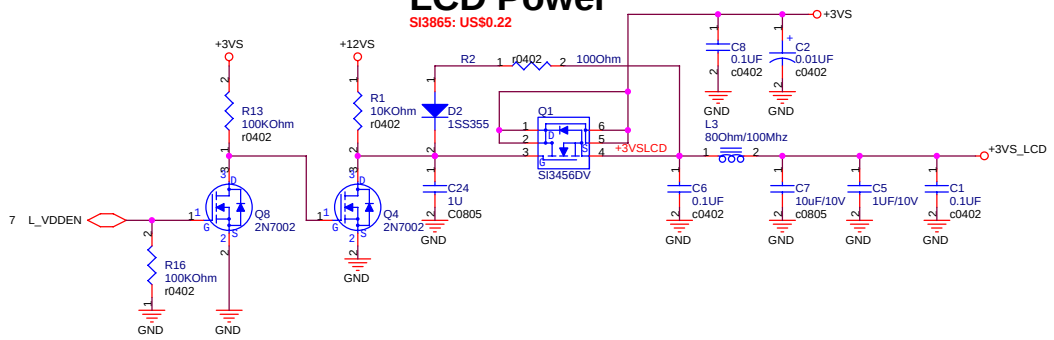
Date: Wednesday, January 26, 2005 Sheet 15 of 50

LCD Backlight Control

LCD Power

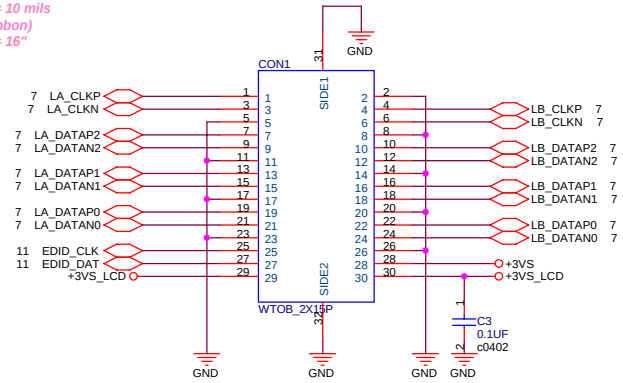
SI3865: US$0.22

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

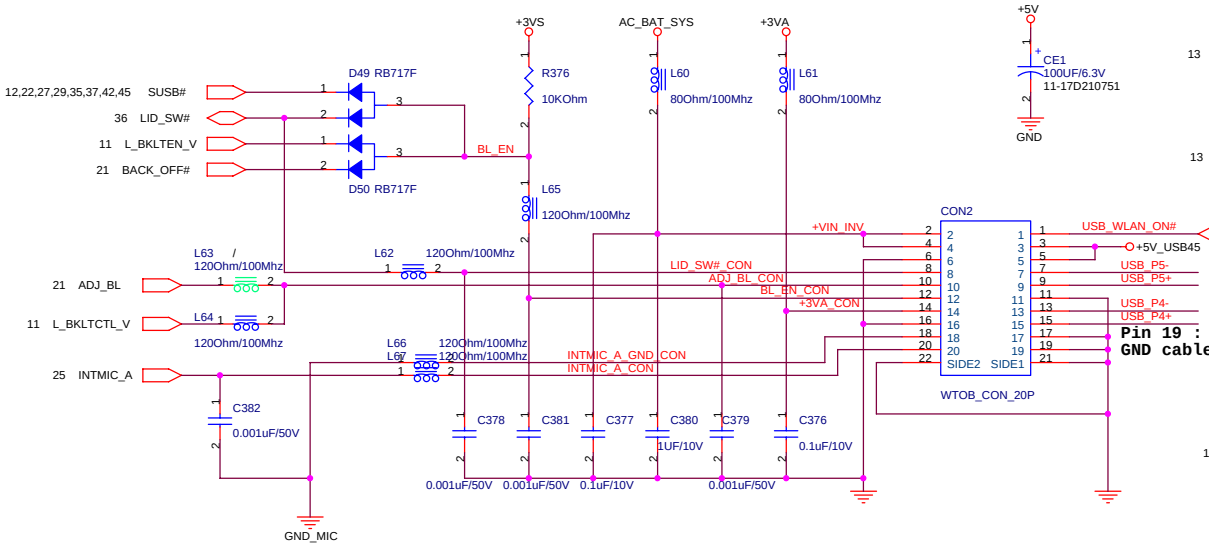


LCD LVDS Interface

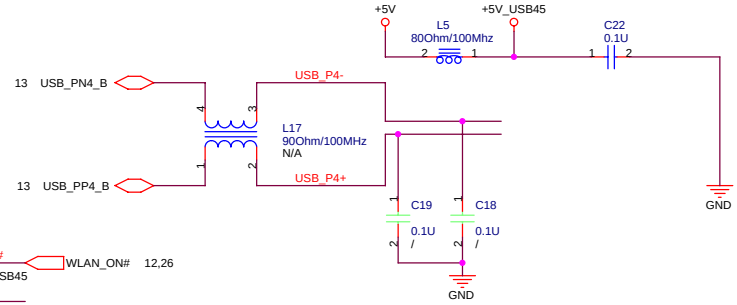
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



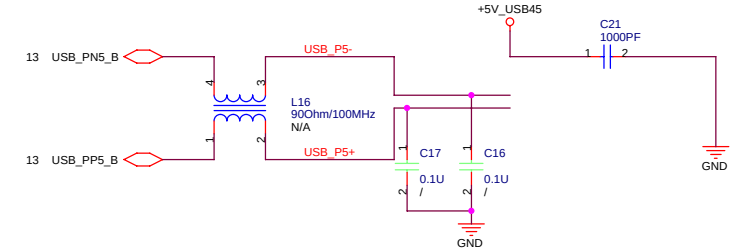
INVERTER Interface



Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



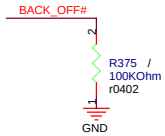
USB PORT 4 for CAMERA



USB PORT 5 for WLAN

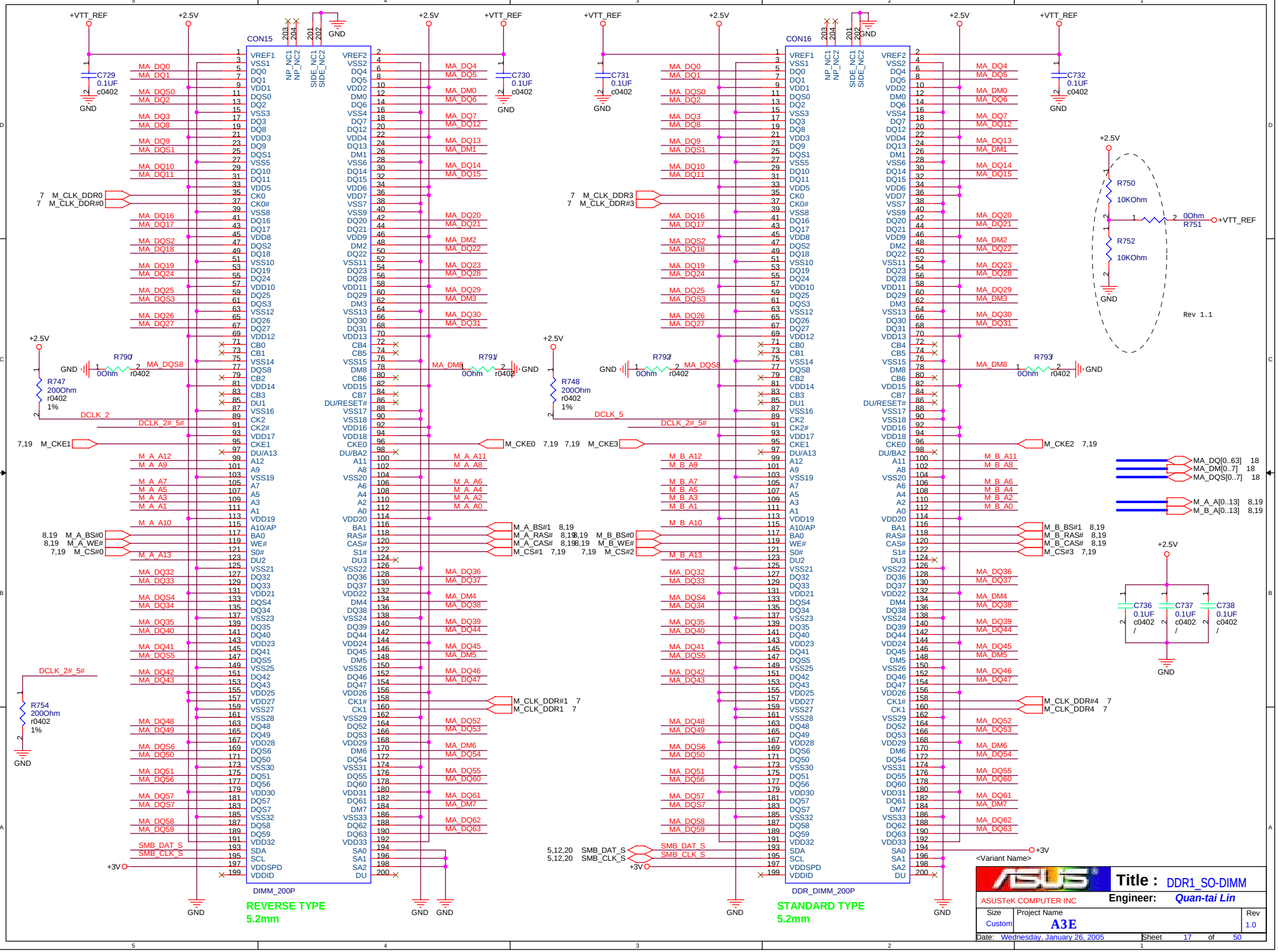
BIOS
ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

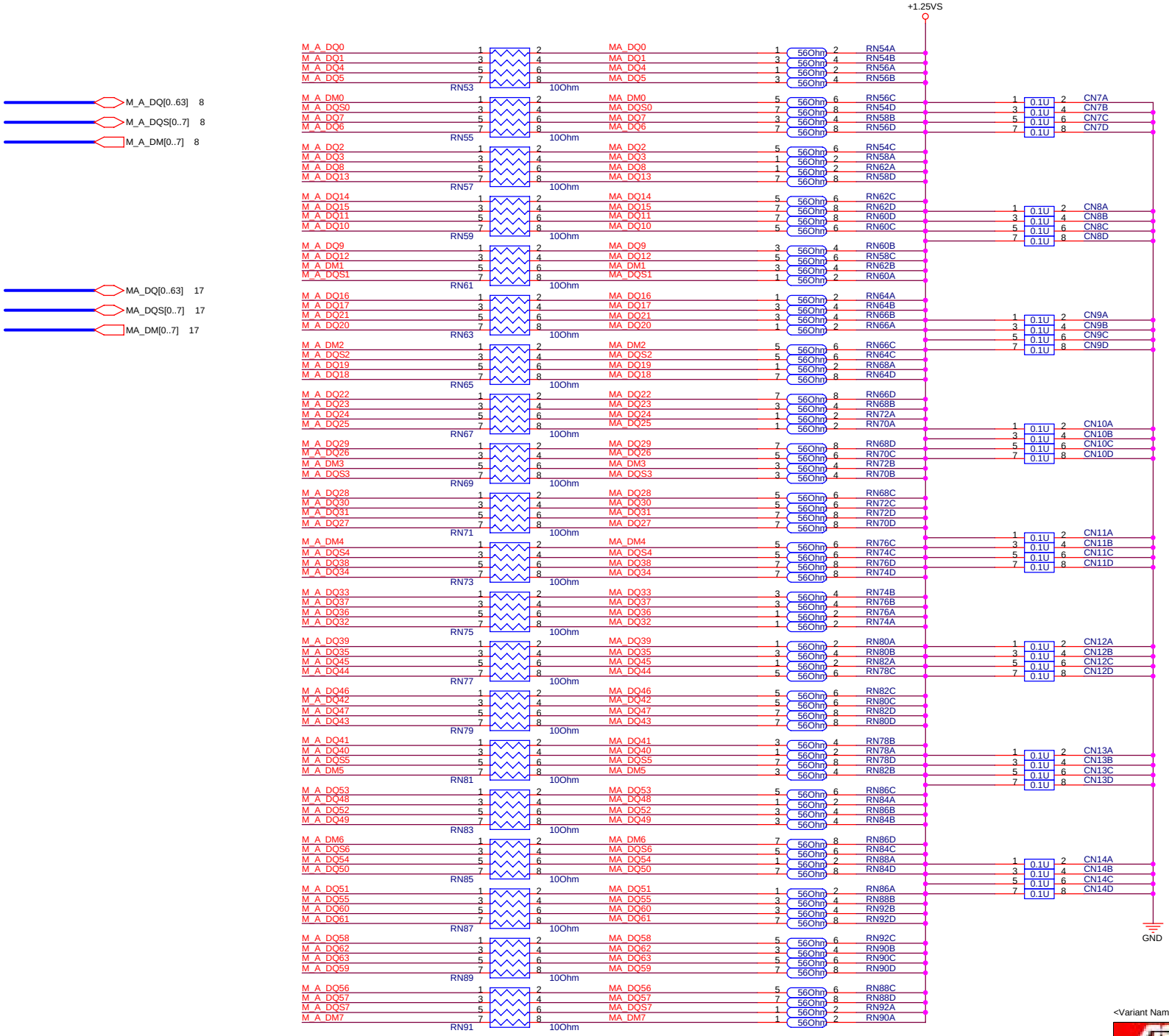
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

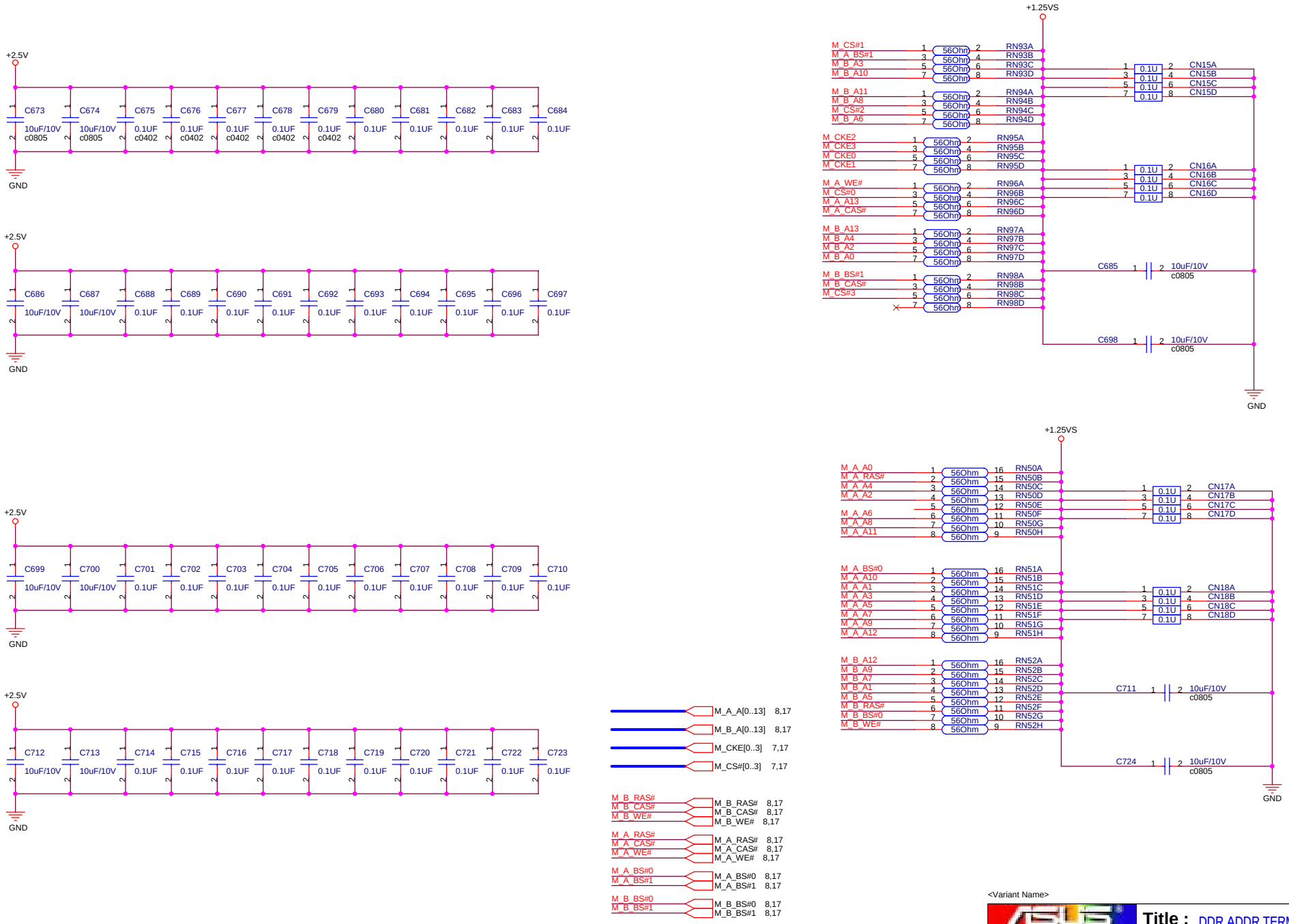
ASUS	Title : LVDS & INVERTER		
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 16 of 50		


CON15
DIMM_200P
REVERSE TYPE
5.2mm
CON16
DDR_DIMM_200P
STANDARD TYPE
5.2mm
+VTT_REF
+2.5V
GND
+3V
C729 0.1UF c0402
C730 0.1UF c0402
C731 0.1UF c0402
C732 0.1UF c0402
R747 200Ohm r0402 1%
R748 200Ohm r0402 1%
R754 200Ohm r0402 1%
R790 0Ohm r0402
R791 0Ohm r0402
R792 0Ohm r0402
R793 0Ohm r0402
R750 10KOhm
R752 10KOhm
R751 0Ohm
Rev 1.1
C736 0.1UF c0402
C737 0.1UF c0402
C738 0.1UF c0402
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR3
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_A_BS#1
M_A_RAS#
M_A_CAS#
M_CS#1
M_B_BS#0
M_B_WE#
M_CS#2
M_B_BS#1
M_B_RAS#
M_B_CAS#
M_CS#3
M_CLK_DDR#1
M_CLK_DDR1
M_CLK_DDR#4
M_CLK_DDR4
SMB_DAT_S
SMB_CLK_S
DCLK_2
DCLK_2#_5#
DCLK_5
MA_DQ[0..63]
MA_DM[0..7]
MA_DQS[0..7]
M_A_A[0..13]
M_B_A[0..13]
ASUSTeK COMPUTER INC
Title : DDR1_SO-DIMM
Engineer: Quan-tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 17 of 50



<Variant Name>

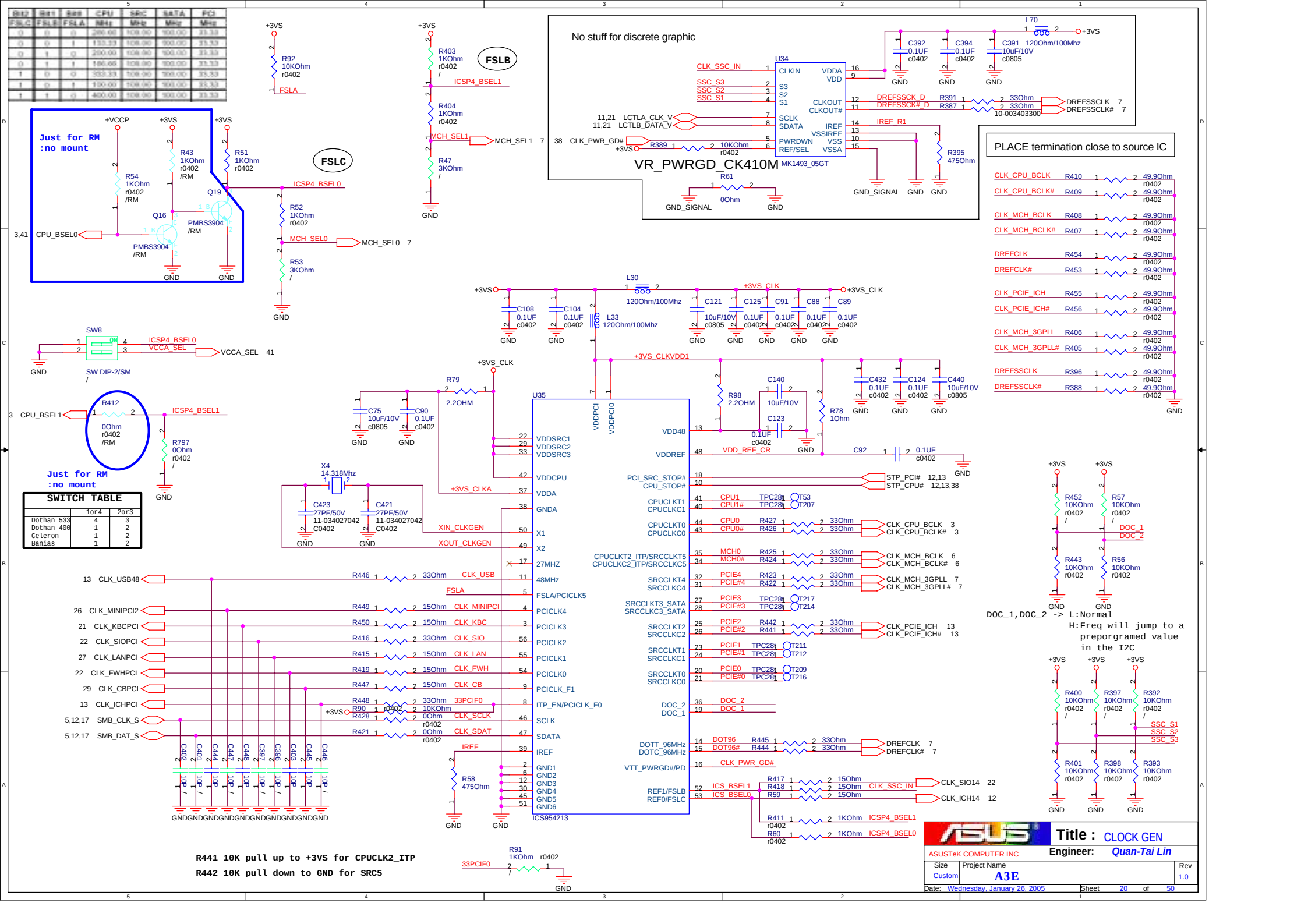
ASUSTeK COMPUTER INC	Title: DDR DATA TERMINATION	Engineer: Quan-tai Lin
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 18 of 50	

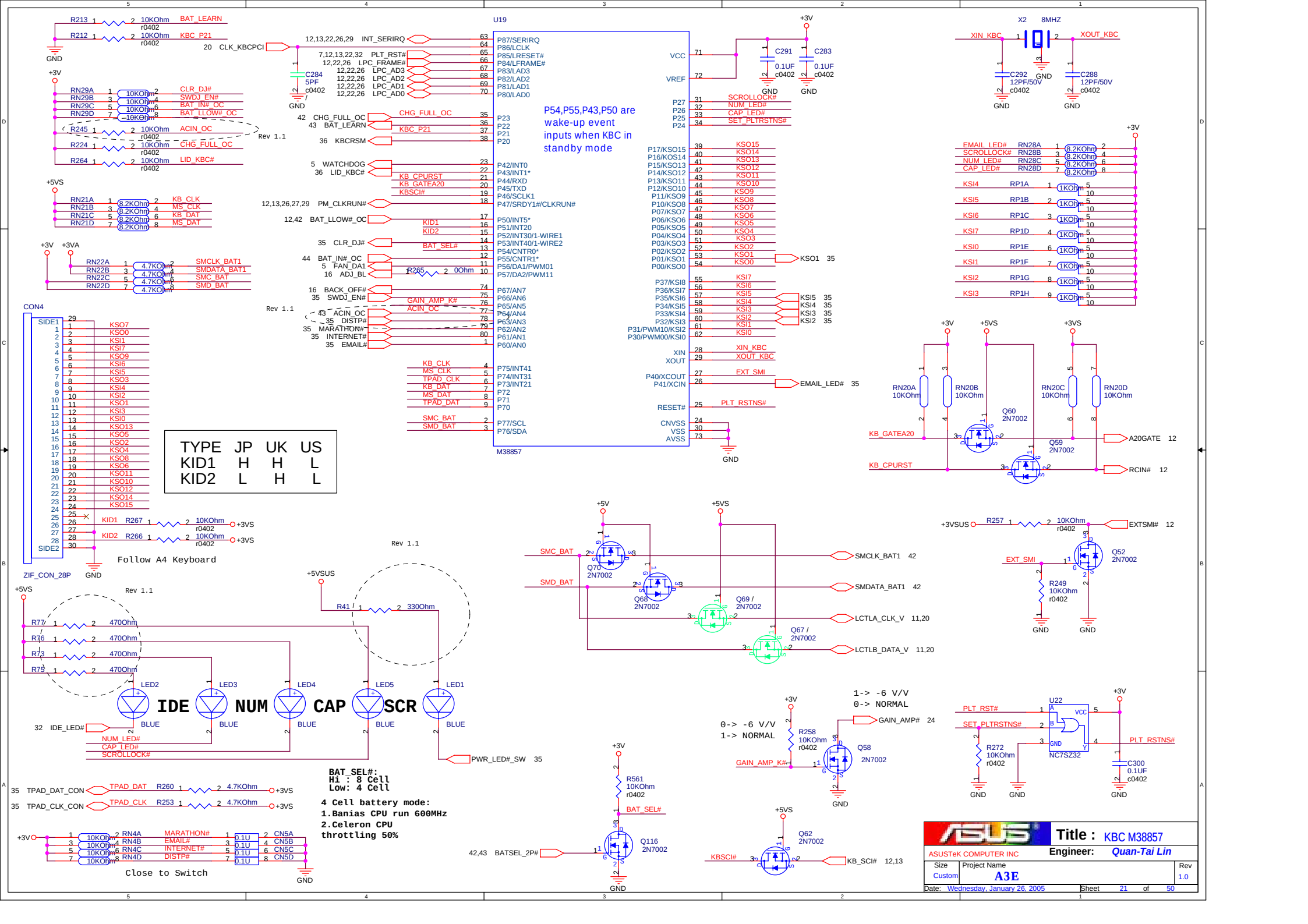


<Variant Name>

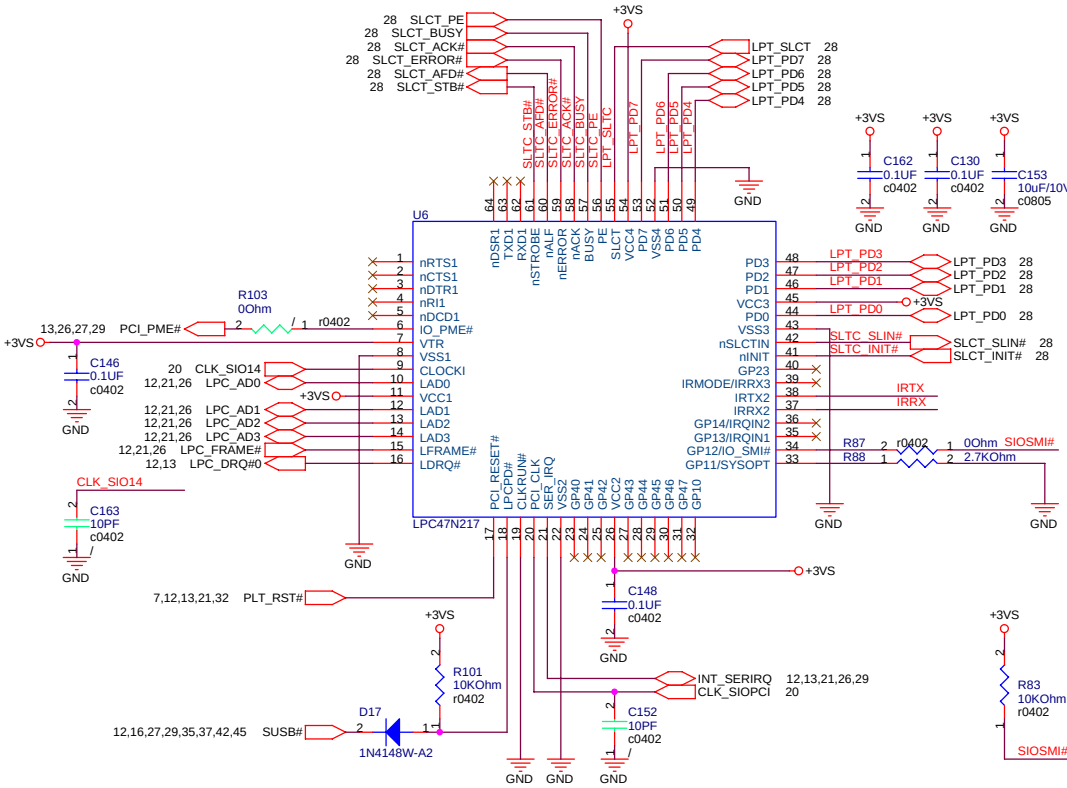
ASUSTeK COMPUTER INC	Title : DDR ADDR TERM	
	Engineer: Quan-tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 19 of 50	

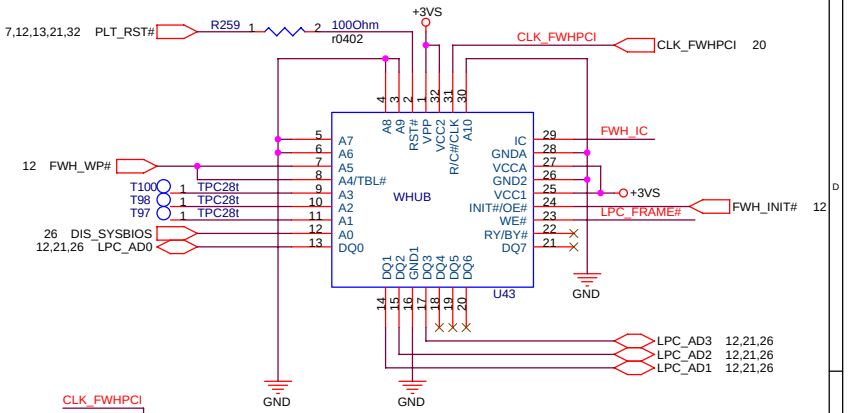
Bit2	Bit1	Bit0	CPU	SRC	SATA	PCI
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	266.66	108.00	100.00	33.33
0	0	1	133.33	108.00	100.00	33.33
0	1	0	200.00	108.00	100.00	33.33
0	1	1	166.66	108.00	100.00	33.33
1	0	0	333.33	108.00	100.00	33.33
1	0	1	100.00	108.00	100.00	33.33
1	1	0	400.00	108.00	100.00	33.33

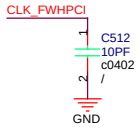



U19
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
X2 8MHZ
XIN_KBC
XOUT_KBC
CON4
ZIF_CON_28P
Follow A4 Keyboard
TYPE JP UK US
KID1 H H L
KID2 L H L
IDE NUM CAP SCR
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
Close to Switch
1-> -6 V/V
0-> NORMAL
0-> -6 V/V
1-> NORMAL
Title : KBC M38857
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 21 of 50

Super I/O

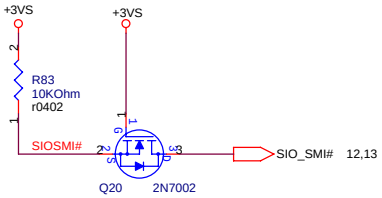






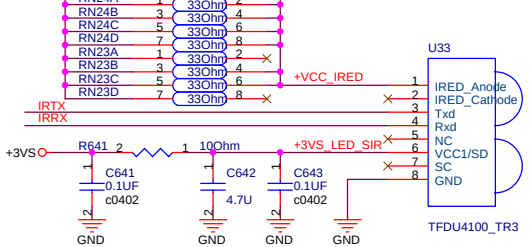
PLCC32 Socket Part Number :
12-043000321

SST FWH/LPC Part Number :
05-001017122(燒)



Keep From Leakage Current

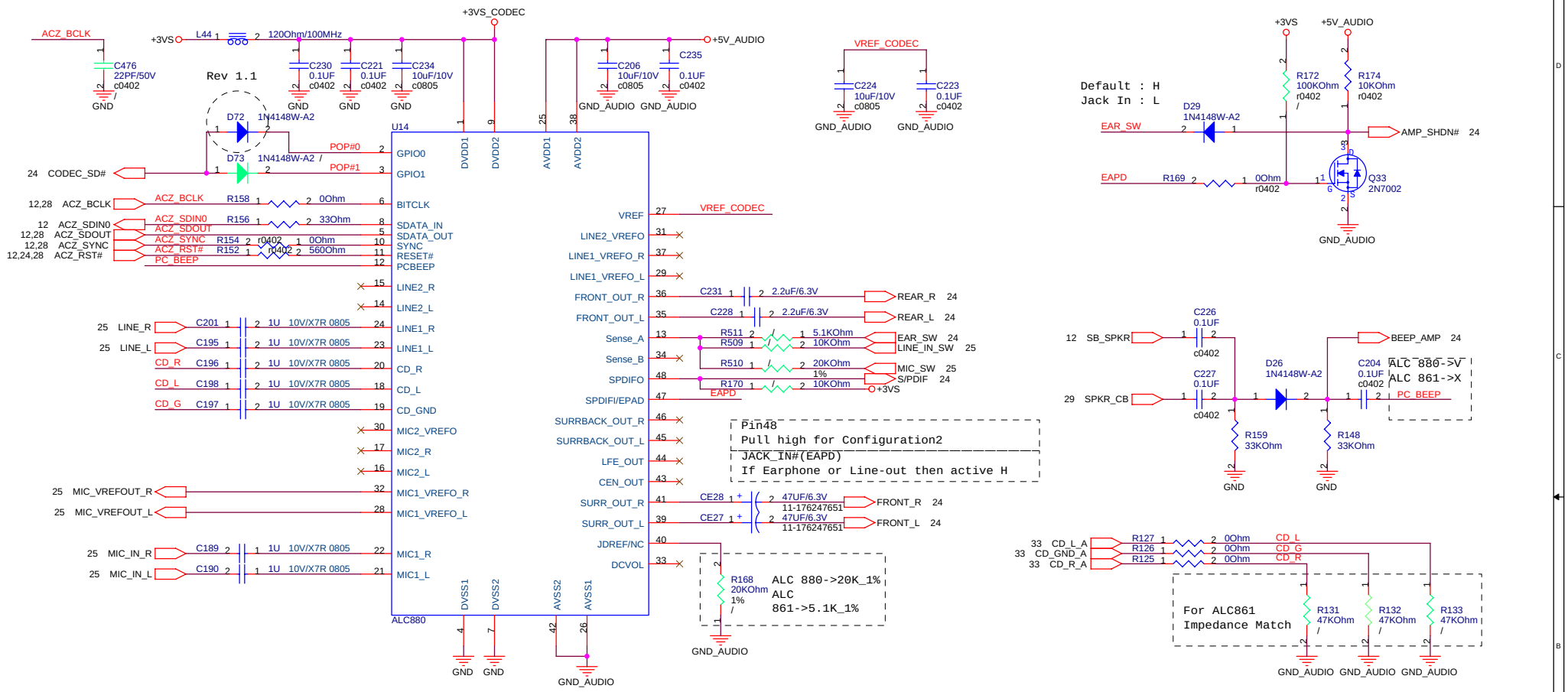
W=35mil

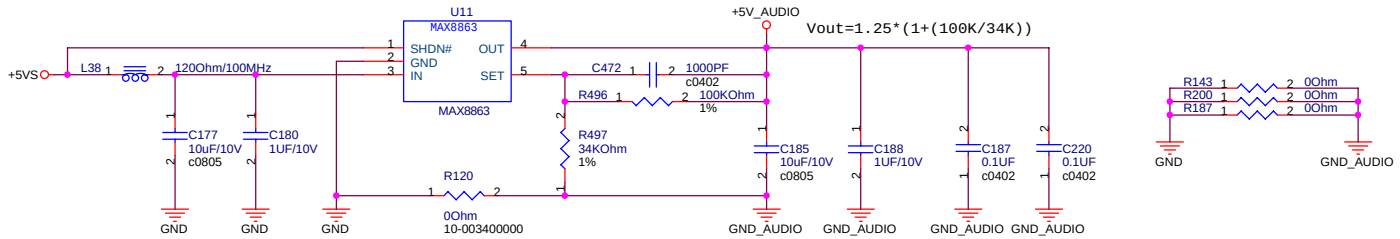


W=35mil

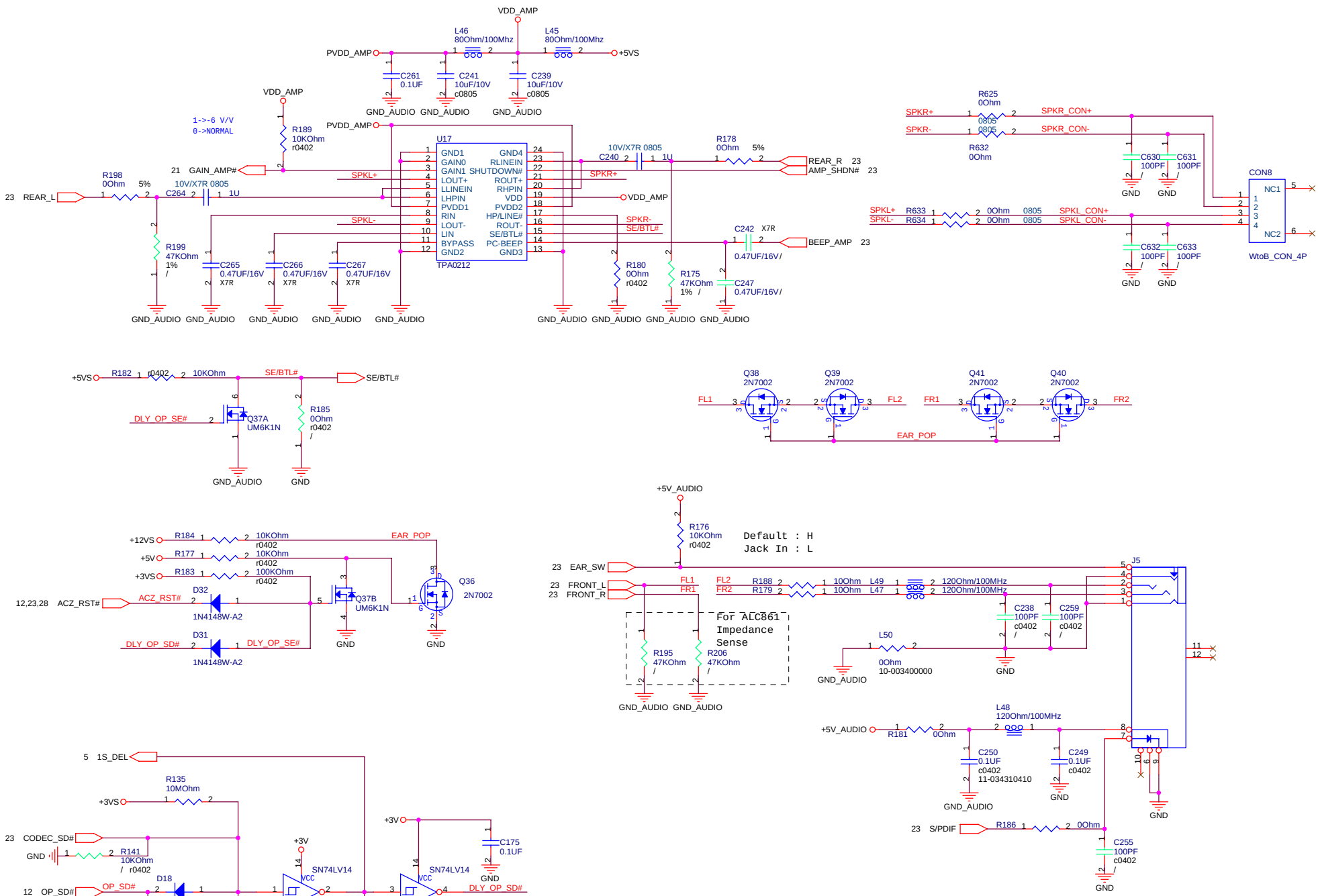
W=20mil

ASUSTeK COMPUTER INC	Title : FWH / SIO / SIR		
	Engineer: *Quan-Tai Lin*		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 22 of 50		

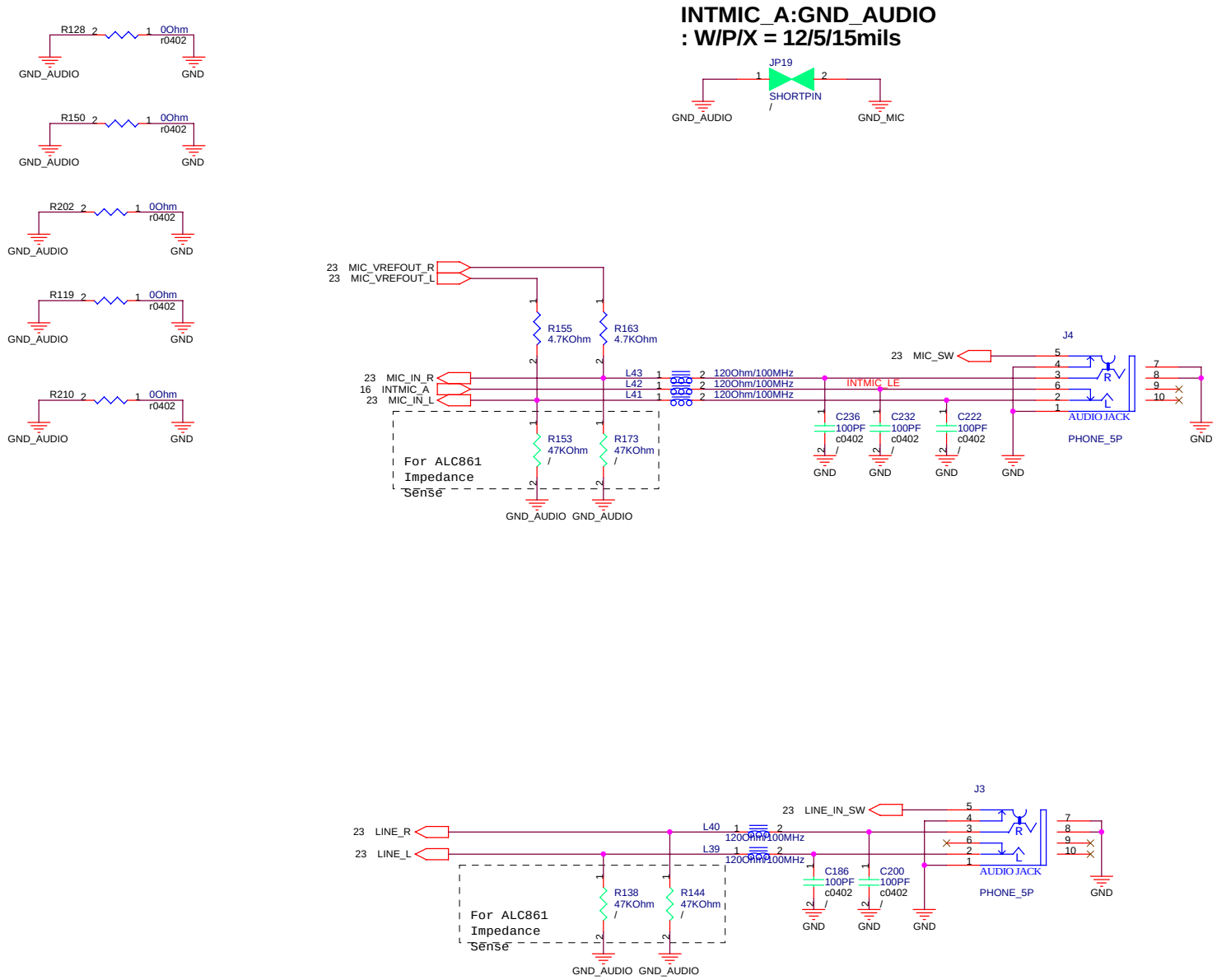




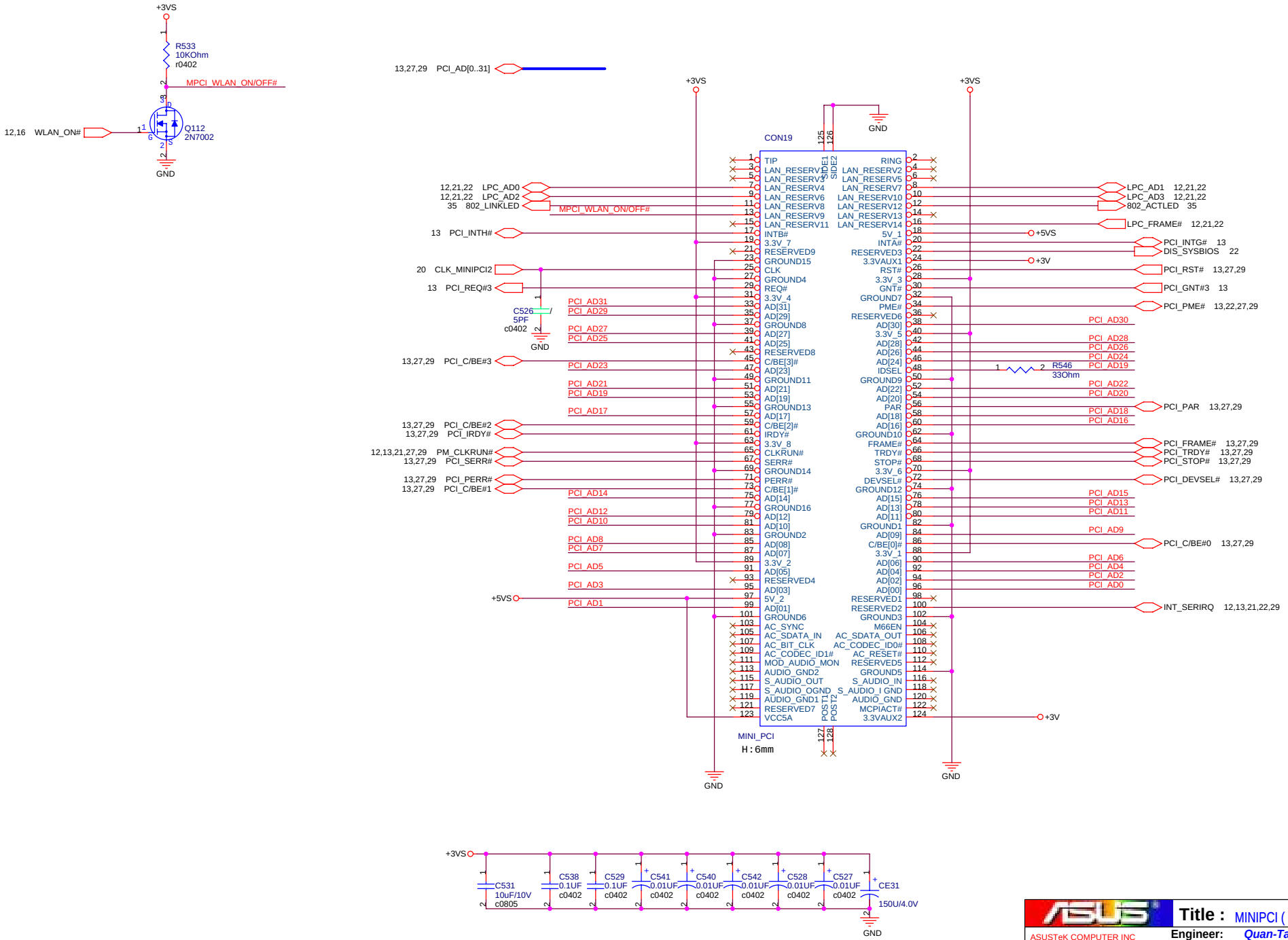
ASUSTek COMPUTER INC. NB1	Title : AZALIA		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 23 of 50		



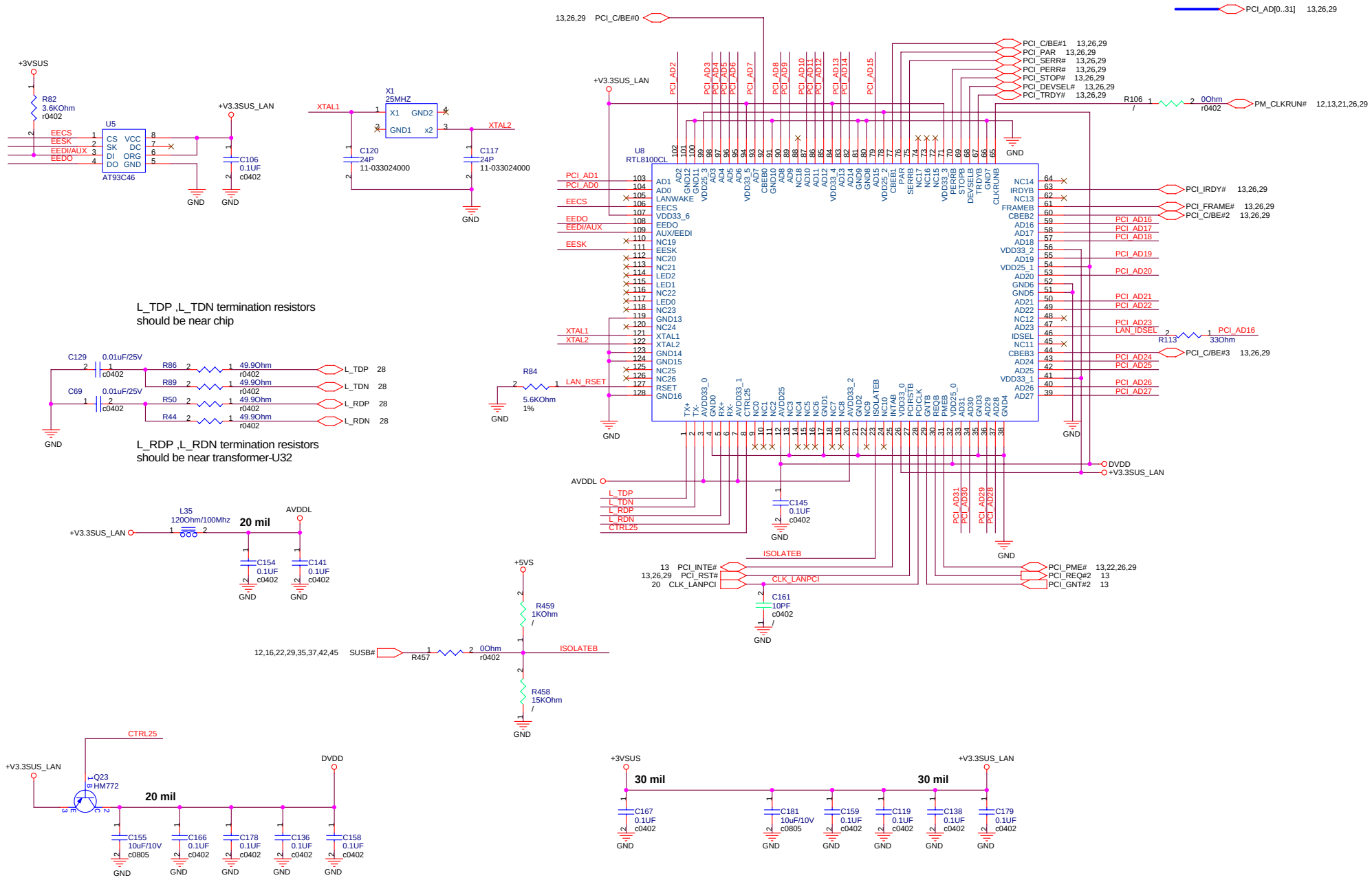
ASUSTeK COMPUTER INC	Title : 2 CHANNEL AMP	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 24 of 50	



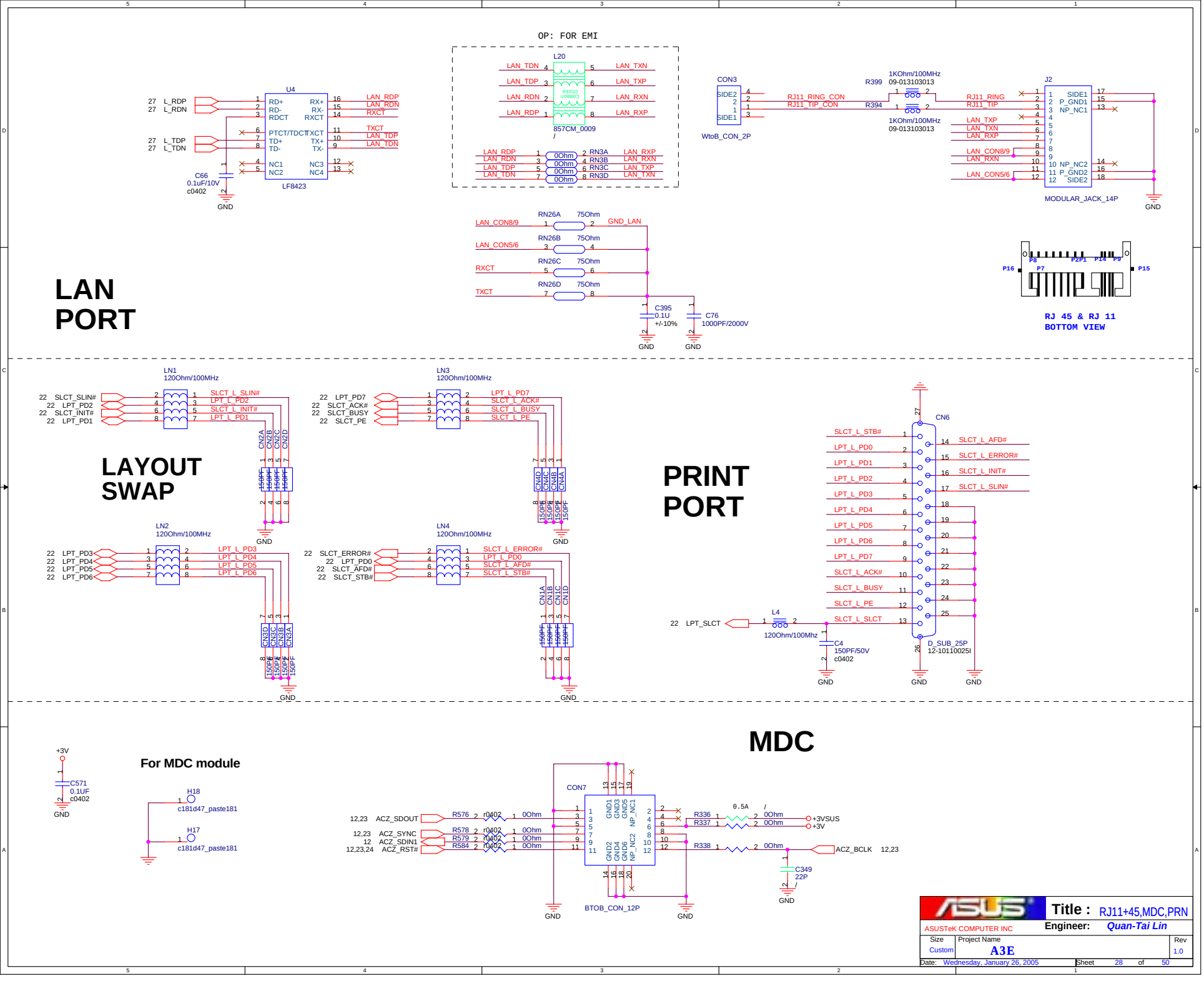
ASUSTeK COMPUTER INC	Title : MIC / Line-IN Jack	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 25 of 50	

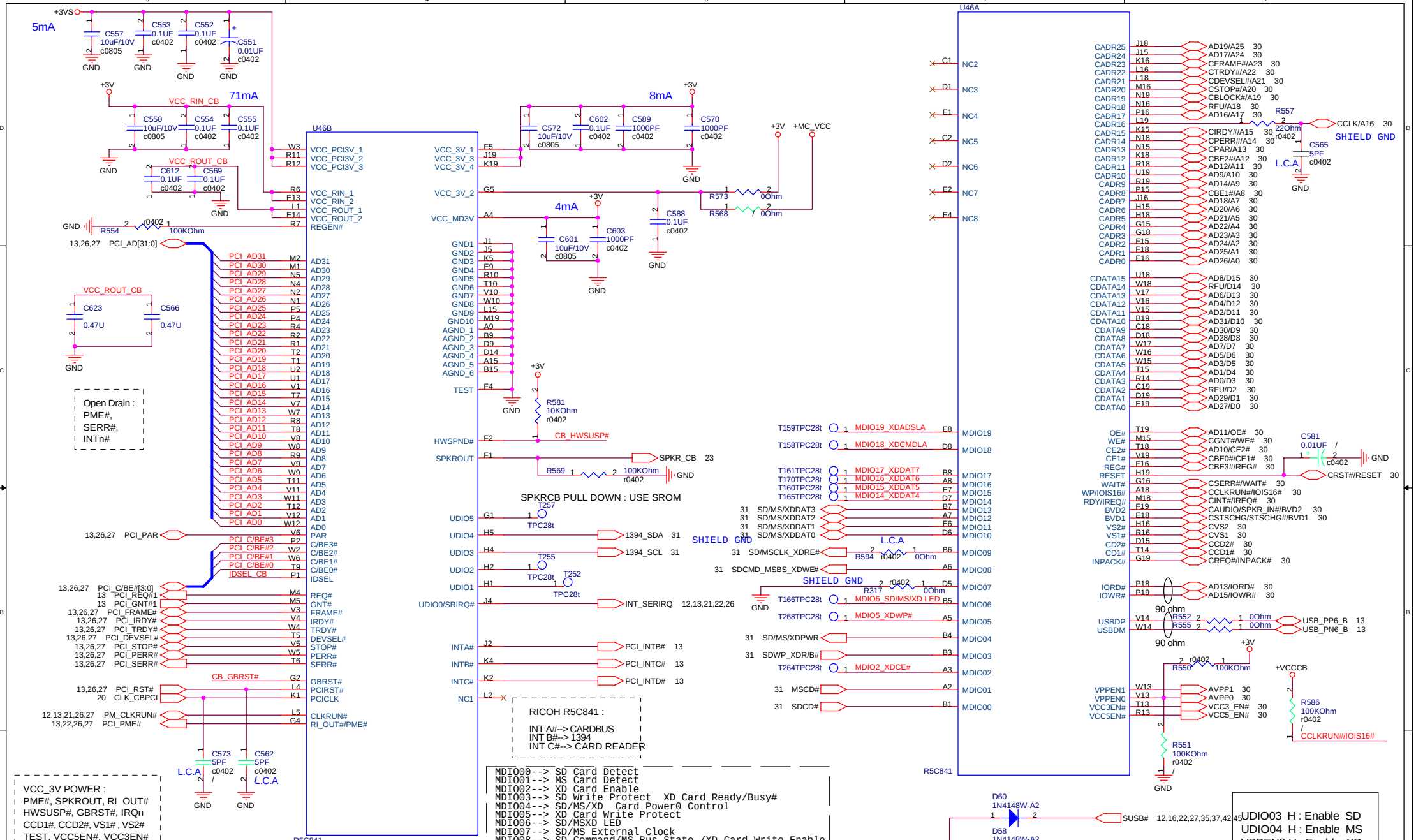


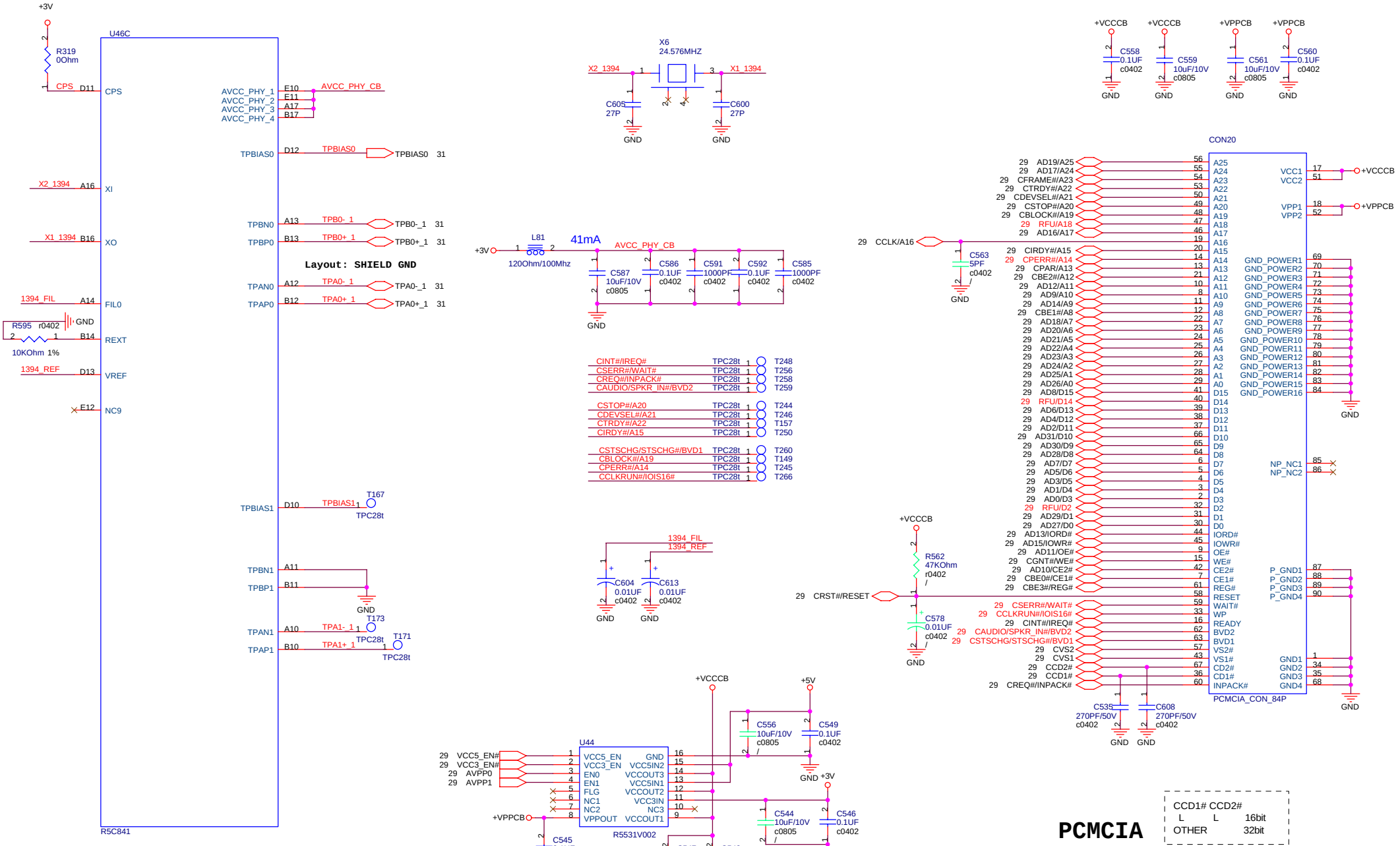
ASUSTeK COMPUTER INC	Title : MINIPCI (802.11)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 26 of 50	

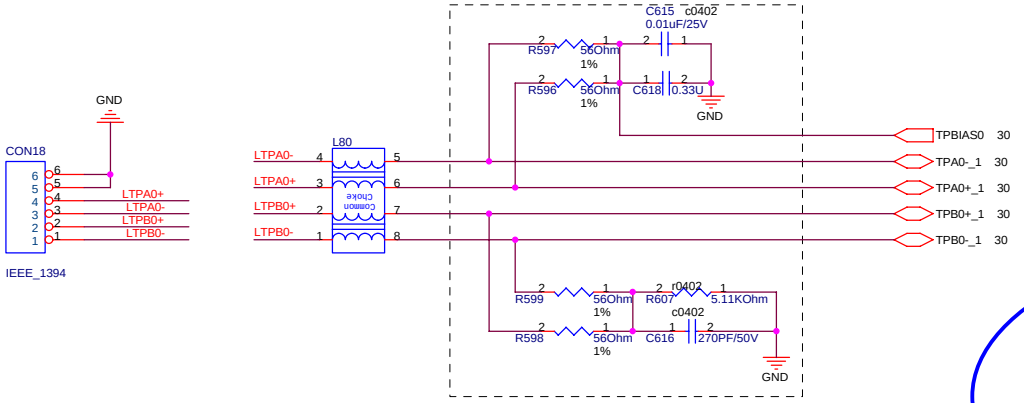


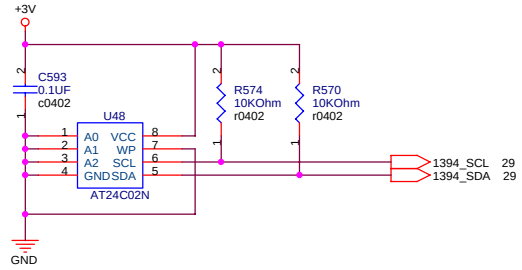
ASUS	Title :	10/100 LAN RTL8100CL
ASUSTeK COMPUTER INC	Engineer:	Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 27 of 50	

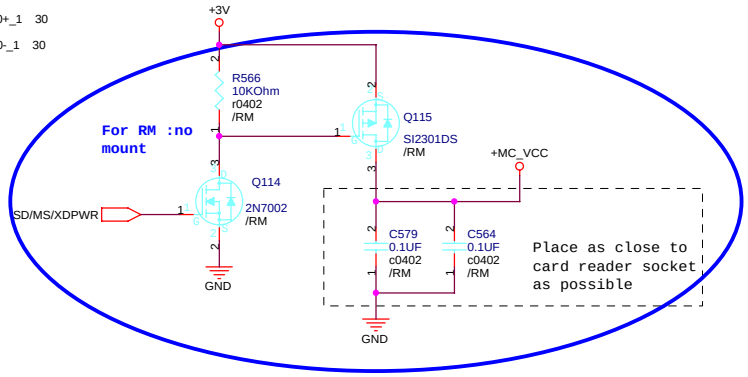

LAN PORT
OP: FOR EMI
U4
LF8423
L20
857CM_0009
CON3
WtoB_CON_2P
J2
MODULAR_JACK_14P
RJ 45 & RJ 11
BOTTOM VIEW
LAYOUT SWAP
PRINT PORT
CN6
D_SUB_25P
12-10110025I
MDC
For MDC module
CON7
BTOB_CON_12P
ASUSTeK COMPUTER INC
Title : RJ11+45,MDC,PRN
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 28 of 50


U46B
U46A
R5C841
5mA
71mA
8mA
4mA
VCC_RIN_CB
VCC_ROUT_CB
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
SHIELD GND
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 29 of 50

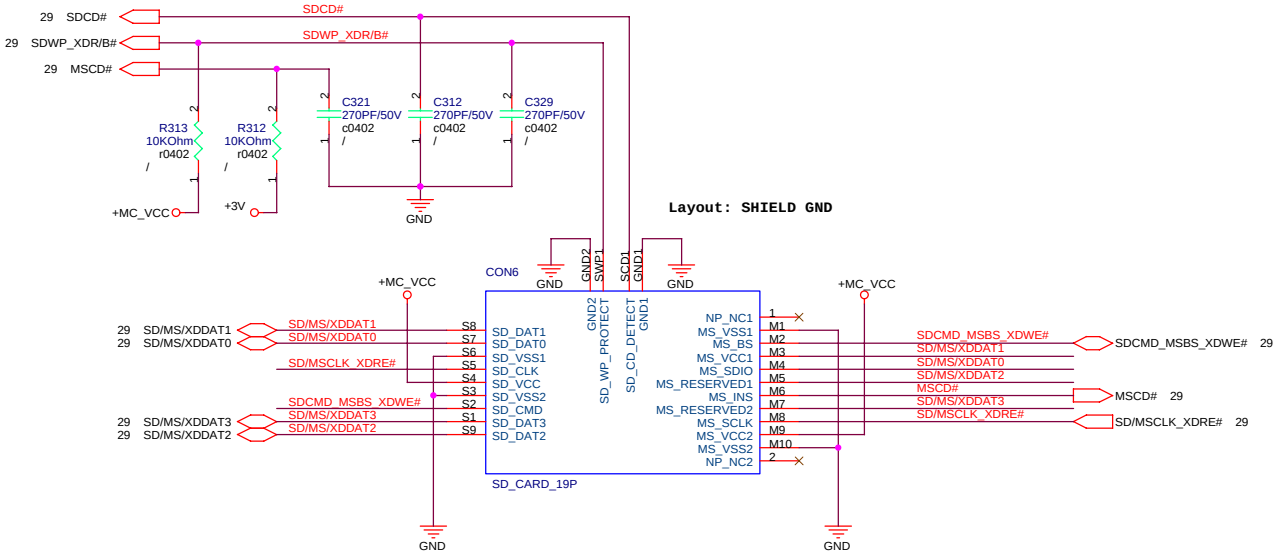

U46C
R5C841
+3V
R319
0Ohm
CPS D11 CPS
AVCC_PHY_1 E10 AVCC_PHY_CB
AVCC_PHY_2 E11
AVCC_PHY_3 A17
AVCC_PHY_4 B17
TPBIAS0 D12 TPBIAS0 TPBIAS0 31
X2_1394 A16 XI
TPBN0 A13 TPB0-_1 TPB0-_1 31
X1_1394 B16 XO
TPBP0 B13 TPB0+_1 TPB0+_1 31
Layout: SHIELD GND
TPAN0 A12 TPA0-_1 TPA0-_1 31
1394_FIL A14 FIL0
TPAP0 B12 TPA0+_1 TPA0+_1 31
R595 r0402 GND
10KOhm 1%
B14 REXT
1394_REF D13 VREF
E12 NC9
TPBIAS1 D10 TPBIAS1 T167 TPC28t
TPBN1 A11
TPBP1 B11
GND
TPAN1 A10 TPA1-_1 T173 TPC28t
TPAP1 B10 TPA1+_1 T171 TPC28t
X6
24.576MHZ
X2_1394 X1_1394
C605 27P
C600 27P
GND
+VCCCB C558 0.1UF c0402
+VCCCB C559 10uF/10V c0805
+VPPCB C561 10uF/10V c0805
+VPPCB C560 0.1UF c0402
+3V L81 120Ohm/100Mhz 41mA AVCC_PHY_CB
C587 10uF/10V c0805
C586 0.1UF c0402
C591 1000PF c0402
C592 0.1UF c0402
C585 1000PF c0402
CINT#/IREQ# TPC28t T248
CSERR#/WAIT# TPC28t T256
CREQ#/INPACK# TPC28t T258
CAUDIO/SPKR_IN#/BVD2 TPC28t T259
CSTOP#/A20 TPC28t T244
CDEVSEL#/A21 TPC28t T246
CTRDY#/A22 TPC28t T157
CIRDY#/A15 TPC28t T250
CSTSCHG/STSCHG#/BVD1 TPC28t T260
CBLOCK#/A19 TPC28t T149
CPERR#/A14 TPC28t T245
CCLKRUN#/IOIS16# TPC28t T266
1394_FIL
1394_REF
C604 0.01UF c0402
C613 0.01UF c0402
CON20
29 AD19/A25
29 AD17/A24
29 CFRAME#/A23
29 CTRDY#/A22
29 CDEVSEL#/A21
29 CSTOP#/A20
29 CBLOCK#/A19
29 RFU/A18
29 AD16/A17
29 CCLK/A16
C563 5PF c0402
29 CIRDY#/A15
29 CPERR#/A14
29 CPAR/A13
29 CBE2#/A12
29 AD12/A11
29 AD9/A10
29 AD14/A9
29 CBE1#/A8
29 AD18/A7
29 AD20/A6
29 AD21/A5
29 AD22/A4
29 AD23/A3
29 AD24/A2
29 AD25/A1
29 AD26/A0
29 AD8/D15
29 RFU/D14
29 AD6/D13
29 AD4/D12
29 AD2/D11
29 AD31/D10
29 AD30/D9
29 AD28/D8
29 AD7/D7
29 AD5/D6
29 AD3/D5
29 AD1/D4
29 AD0/D3
29 RFU/D2
29 AD29/D1
29 AD27/D0
29 AD13/IORD#
29 AD15/IOWR#
29 AD11/OE#
29 CGNT#/WE#
29 AD10/CE2#
29 CBE0#/CE1#
29 CBE3#/REG#
29 CSERR#/WAIT#
29 CCLKRUN#/IOIS16#
29 CINT#/IREQ#
29 CAUDIO/SPKR_IN#/BVD2
29 CSTSCHG/STSCHG#/BVD1
29 CVS2
29 CVS1
29 CCD2#
29 CCD1#
29 CREQ#/INPACK#
VCC1 VCC2 +VCCCB
VPP1 VPP2 +VPPCB
GND_POWER1 GND_POWER2 GND_POWER3 GND_POWER4 GND_POWER5 GND_POWER6 GND_POWER7 GND_POWER8 GND_POWER9 GND_POWER10 GND_POWER11 GND_POWER12 GND_POWER13 GND_POWER14 GND_POWER15 GND_POWER16
NP_NC1 NP_NC2
P_GND1 P_GND2 P_GND3 P_GND4
GND1 GND2 GND3 GND4
PCMCIA_CON_84P
+VCCCB
R562 47KOhm r0402
29 CRST#/RESET
C578 0.01UF c0402
C535 270PF/50V c0402
C608 270PF/50V c0402
U44
R5531V002
29 VCC5_EN#
29 VCC3_EN#
29 AVPP0
29 AVPP1
VCC5_EN VCC3_EN EN0 EN1 FLG NC1 NC2 VPPOUT
GND VCC5IN2 VCCOUT3 VCC5IN1 VCCOUT2 VCC3IN NC3 VCCOUT1
+VPPCB
+VCCCB
+5V
C556 10uF/10V c0805
C549 0.1UF c0402
+3V
C544 10uF/10V c0805
C546 0.1UF c0402
C545 0.1UF c0402
C547 0.1UF c0402
C548 0.1UF c0402
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 30 of 50



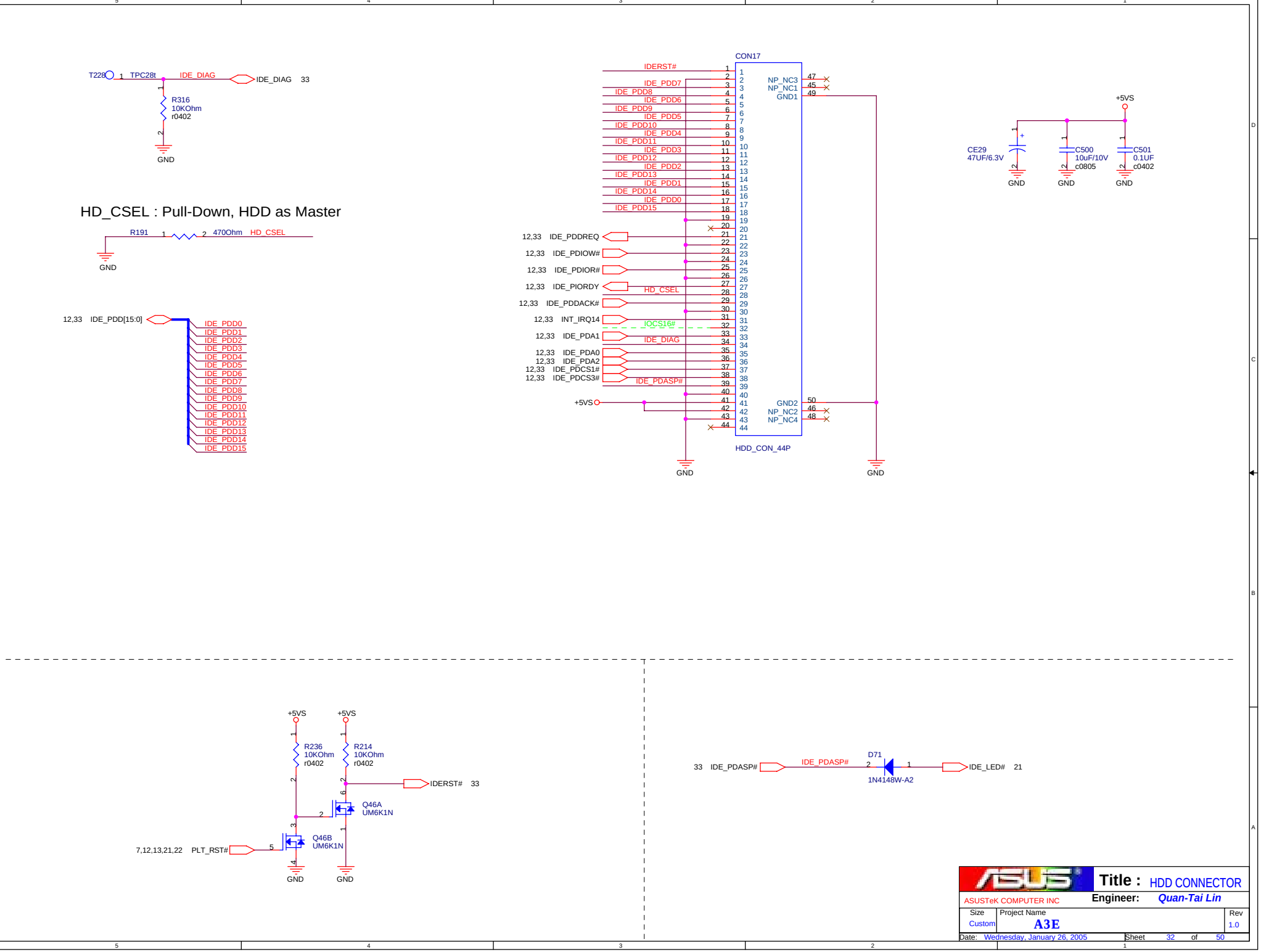


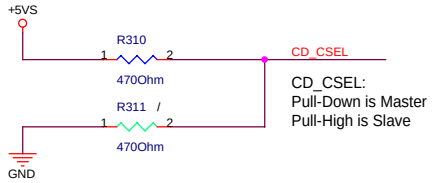


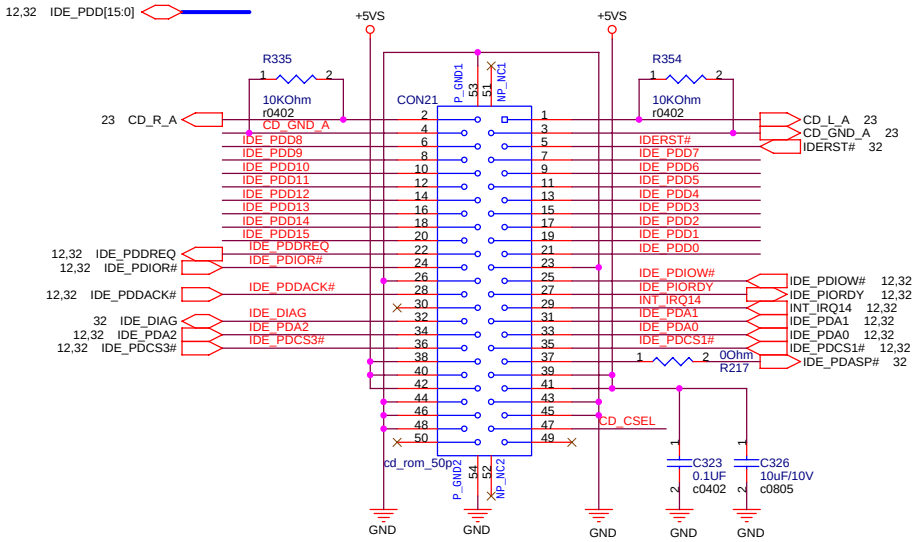
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

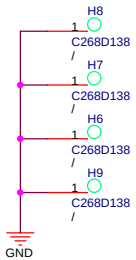


ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON		
	Engineer: Quan-Tai Lin		
Size Custom	Project Name A3E		Rev 1.0
Date: Wednesday, January 26, 2005	Sheet 31 of 50		

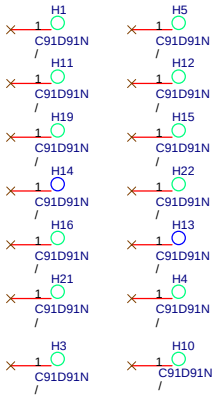

T228
TPC28t
IDE_DIAG
IDE_DIAG 33
R316
10KOhm
r0402
GND
HD_CSEL : Pull-Down, HDD as Master
R191
470Ohm
HD_CSEL
GND
12,33 IDE_PDD[15:0]
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
CON17
IDERST#
IDE_PDD7
IDE_PDD8
IDE_PDD6
IDE_PDD9
IDE_PDD5
IDE_PDD10
IDE_PDD4
IDE_PDD11
IDE_PDD3
IDE_PDD12
IDE_PDD2
IDE_PDD13
IDE_PDD1
IDE_PDD14
IDE_PDD0
IDE_PDD15
12,33 IDE_PDDREQ
12,33 IDE_PDIOW#
12,33 IDE_PDIOR#
12,33 IDE_PIORDY
HD_CSEL
12,33 IDE_PDDACK#
12,33 INT_IRQ14
IOCS16#
12,33 IDE_PDA1
IDE_DIAG
12,33 IDE_PDA0
12,33 IDE_PDA2
12,33 IDE_PDCS1#
12,33 IDE_PDCS3#
IDE_PDASP#
+5VS
NP_NC3
NP_NC1
GND1
GND2
NP_NC2
NP_NC4
HDD_CON_44P
GND
GND
+5VS
CE29
47UF/6.3V
C500
10uF/10V
c0805
C501
0.1UF
c0402
GND
GND
GND
+5VS
+5VS
R236
10KOhm
r0402
R214
10KOhm
r0402
IDERST# 33
Q46A
UM6K1N
Q46B
UM6K1N
7,12,13,21,22 PLT_RST#
GND
GND
33 IDE_PDASP#
IDE_PDASP#
D71
1N4148W-A2
IDE_LED# 21
ASUSTeK COMPUTER INC
Title : HDD CONNECTOR
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 32 of 50

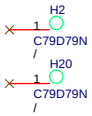


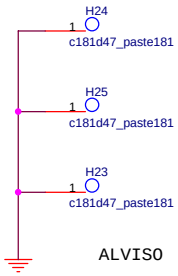




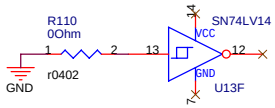
CPU

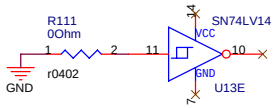






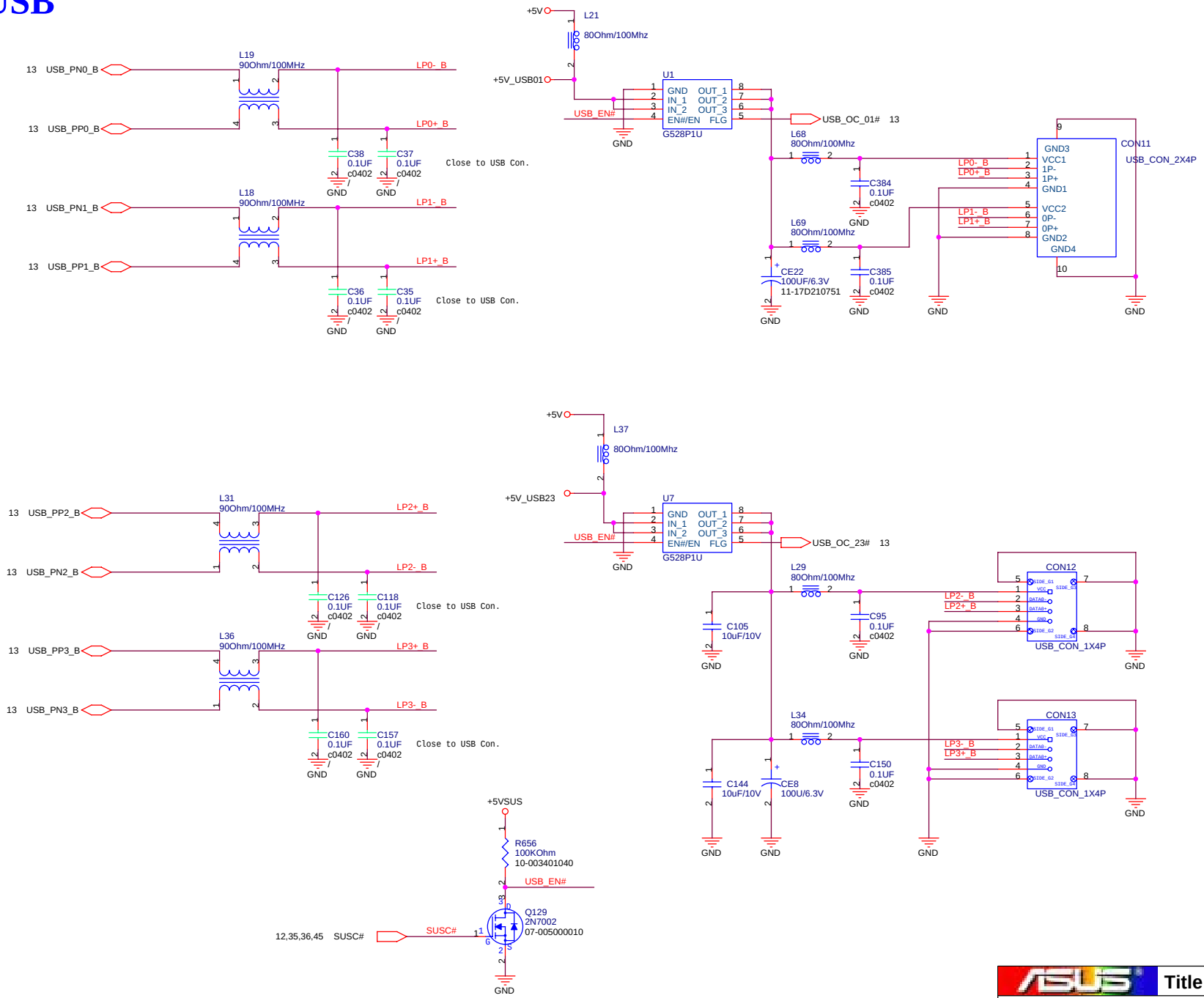
ALVISO



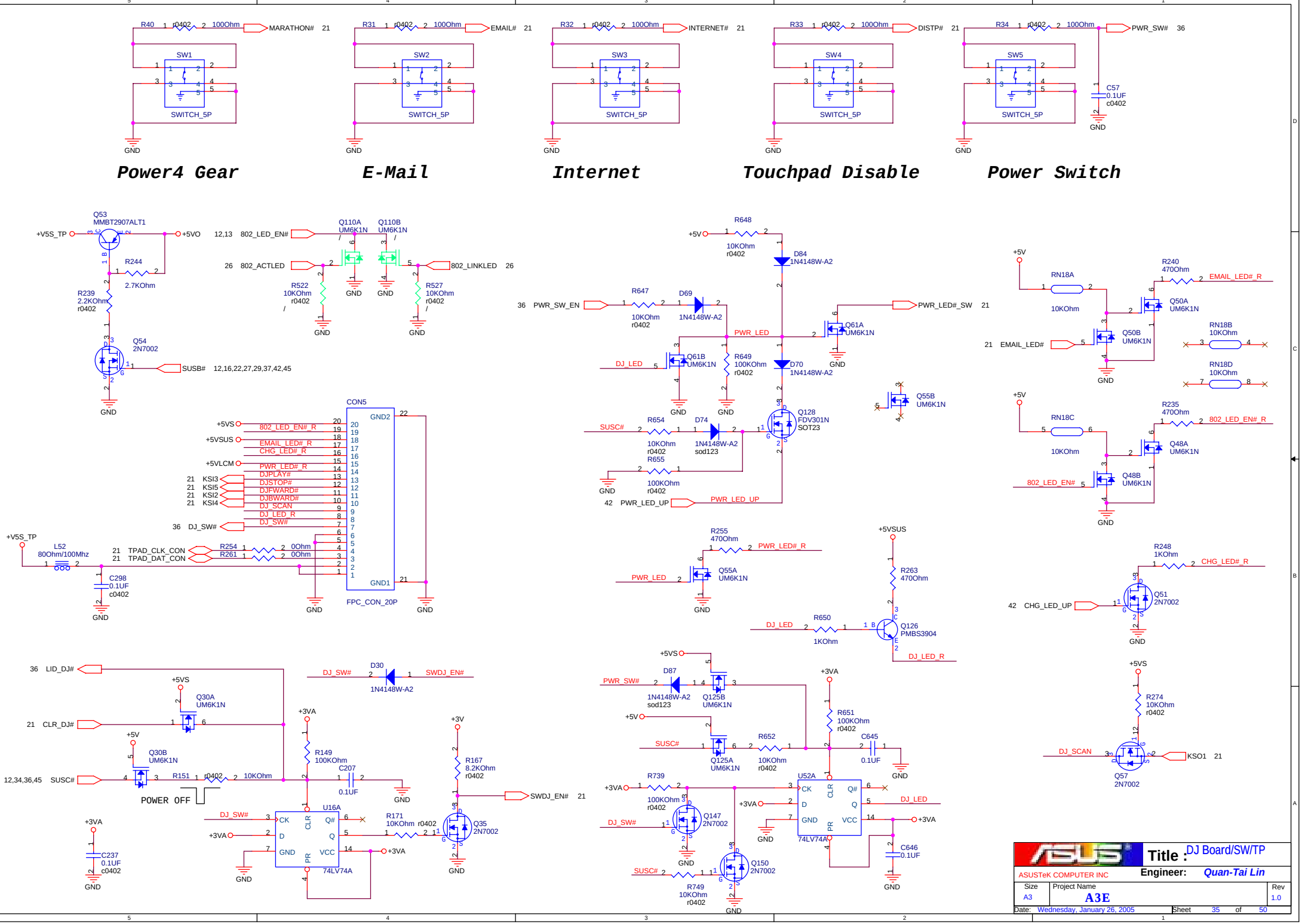


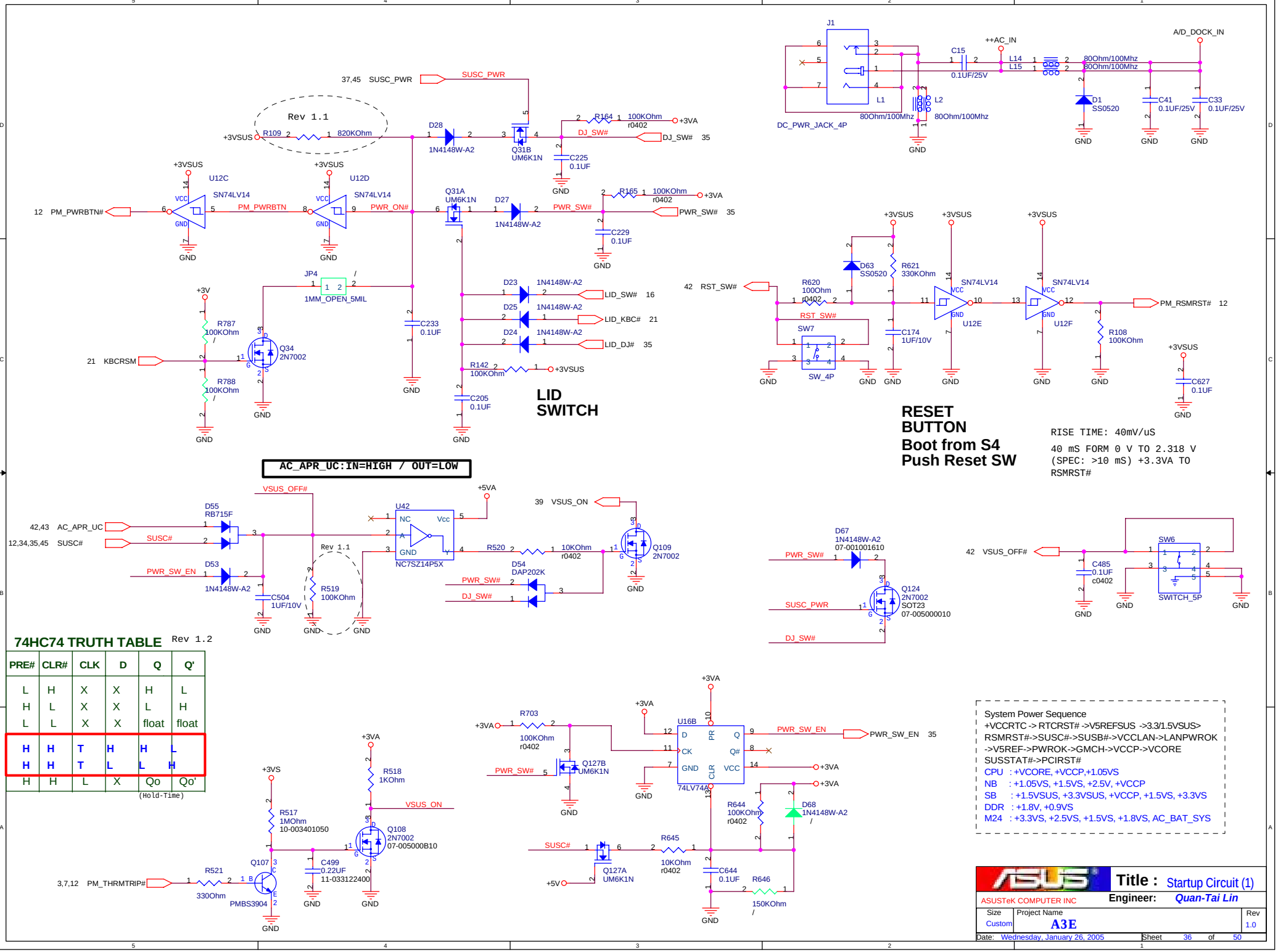
ASUSTeK COMPUTER INC	Title : CDROM	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 33 of 50	

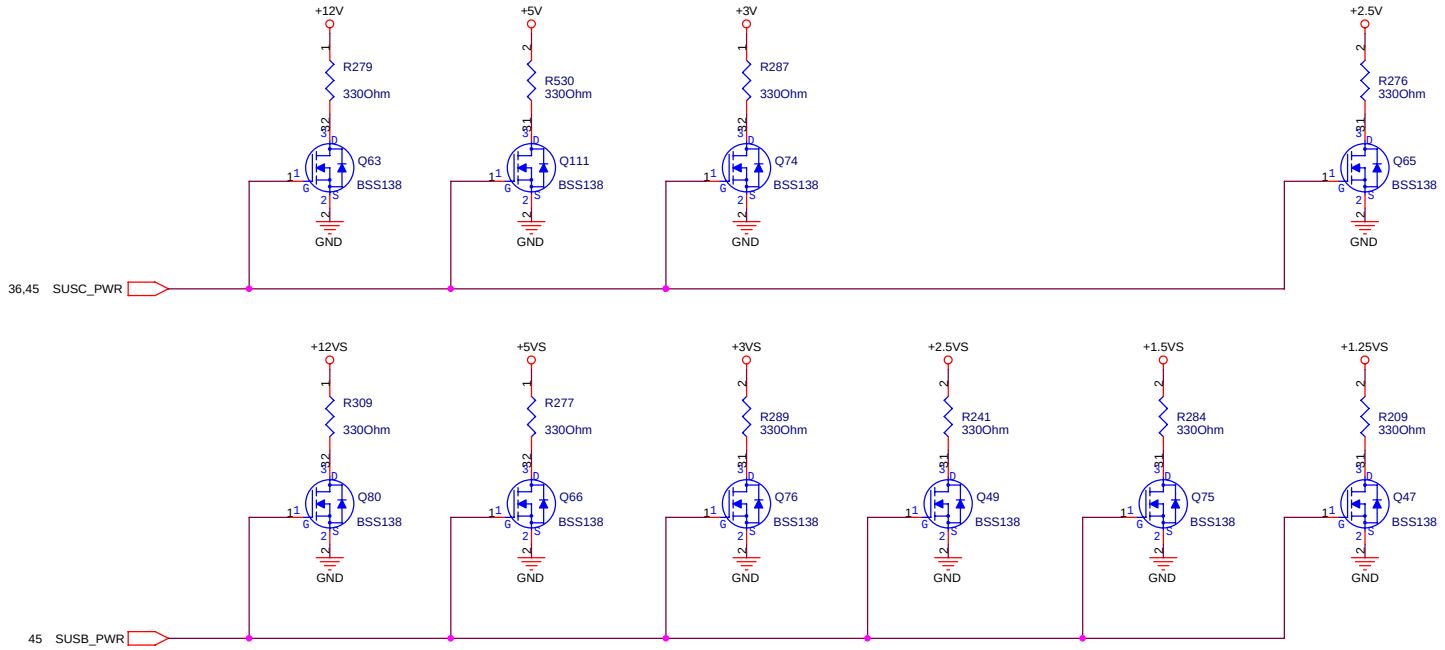
USB



ASUSTeK COMPUTER INC	Title : USB CONN	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 34 of 50	

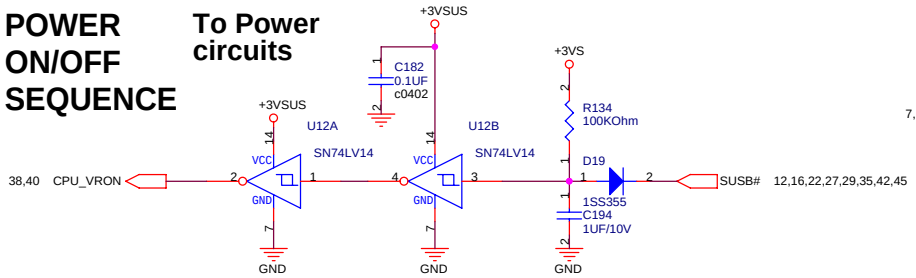

Power4 Gear
E-Mail
Internet
Touchpad Disable
Power Switch
MARATHON# 21
EMAIL# 21
INTERNET# 21
DISTP# 21
PWR_SW# 36
SWITCH_5P
GND
Q53 MMBT2907ALT1
+V5S_TP
+5VO
R244 2.7KOhm
R239 2.2KOhm r0402
Q54 2N7002
SUSB# 12,16,22,27,29,37,42,45
12,13 802_LED_EN#
26 802_ACTLED
802_LINKLED 26
Q110A UM6K1N
Q110B UM6K1N
R522 10KOhm r0402
R527 10KOhm r0402
CON5
FPC_CON_20P
+5VS
+5VSUS
+5VLCM
802_LED_EN#_R
EMAIL_LED#_R
CHG_LED#_R
PWR_LED#_R
DJPLAY#
DJSTOP#
DJFWARD#
DJBWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
21 KSI3
21 KSI5
21 KSI2
21 KSI4
36 DJ_SW#
L52 80Ohm/100Mhz
C298 0.1UF c0402
21 TPAD_CLK_CON
21 TPAD_DAT_CON
R254 0Ohm
R261 0Ohm
36 LID_DJ#
21 CLR_DJ#
Q30A UM6K1N
Q30B UM6K1N
12,34,36,45 SUSC#
R151 r0402 10KOhm
POWER OFF
DJ_SW#
D30 1N4148W-A2
SWDJ_EN#
R149 100KOhm
C207 0.1UF
U16A
74LV74A
R171 10KOhm r0402
R167 8.2KOhm r0402
Q35 2N7002
SWDJ_EN# 21
C237 0.1UF c0402
R648 10KOhm r0402
D84 1N4148W-A2
36 PWR_SW_EN
R647 10KOhm r0402
D69 1N4148W-A2
PWR_LED
PWR_LED#_SW 21
Q61A UM6K1N
DJ_LED
Q61B UM6K1N
R649 100KOhm r0402
D70 1N4148W-A2
Q55B UM6K1N
SUSC#
R654 10KOhm r0402
D74 1N4148W-A2 sod123
Q128 FDV301N SOT23
R655 100KOhm r0402
42 PWR_LED_UP
PWR_LED_UP
R255 470Ohm
PWR_LED#_R
Q55A UM6K1N
+5VSUS
R263 470Ohm
R650 1KOhm
Q126 PMBS3904
DJ_LED_R
PWR_SW#
D87 1N4148W-A2 sod123
Q125B UM6K1N
Q125A UM6K1N
R652 10KOhm r0402
R651 100KOhm r0402
C645 0.1UF
R739 100KOhm r0402
Q147 2N7002
U52A
74LV74A
C646 0.1UF
R749 10KOhm r0402
Q150 2N7002
RN18A 10KOhm
R240 470Ohm
EMAIL_LED#_R
Q50A UM6K1N
Q50B UM6K1N
21 EMAIL_LED#
RN18B 10KOhm
RN18D 10KOhm
RN18C 10KOhm
R235 470Ohm
802_LED_EN#_R
Q48A UM6K1N
Q48B UM6K1N
802_LED_EN#
R248 1KOhm
CHG_LED#_R
Q51 2N7002
42 CHG_LED_UP
R274 10KOhm r0402
DJ_SCAN
KSO1 21
Q57 2N7002
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size A3
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 35 of 50

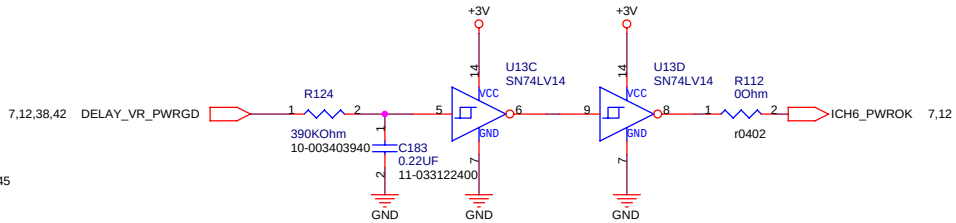

LID SWITCH
RESET BUTTON
Boot from S4
Push Reset SW
RISE TIME: 40mV/uS
40 mS FORM 0 V TO 2.318 V (SPEC: >10 mS) +3.3VA TO RSMRST#
AC_APR_UC:IN=HIGH / OUT=LOW
74HC74 TRUTH TABLE Rev 1.2
System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.5VS, +2.5V, +VCCP
SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS
M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS
Title : Startup Circuit (1)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 36 of 50



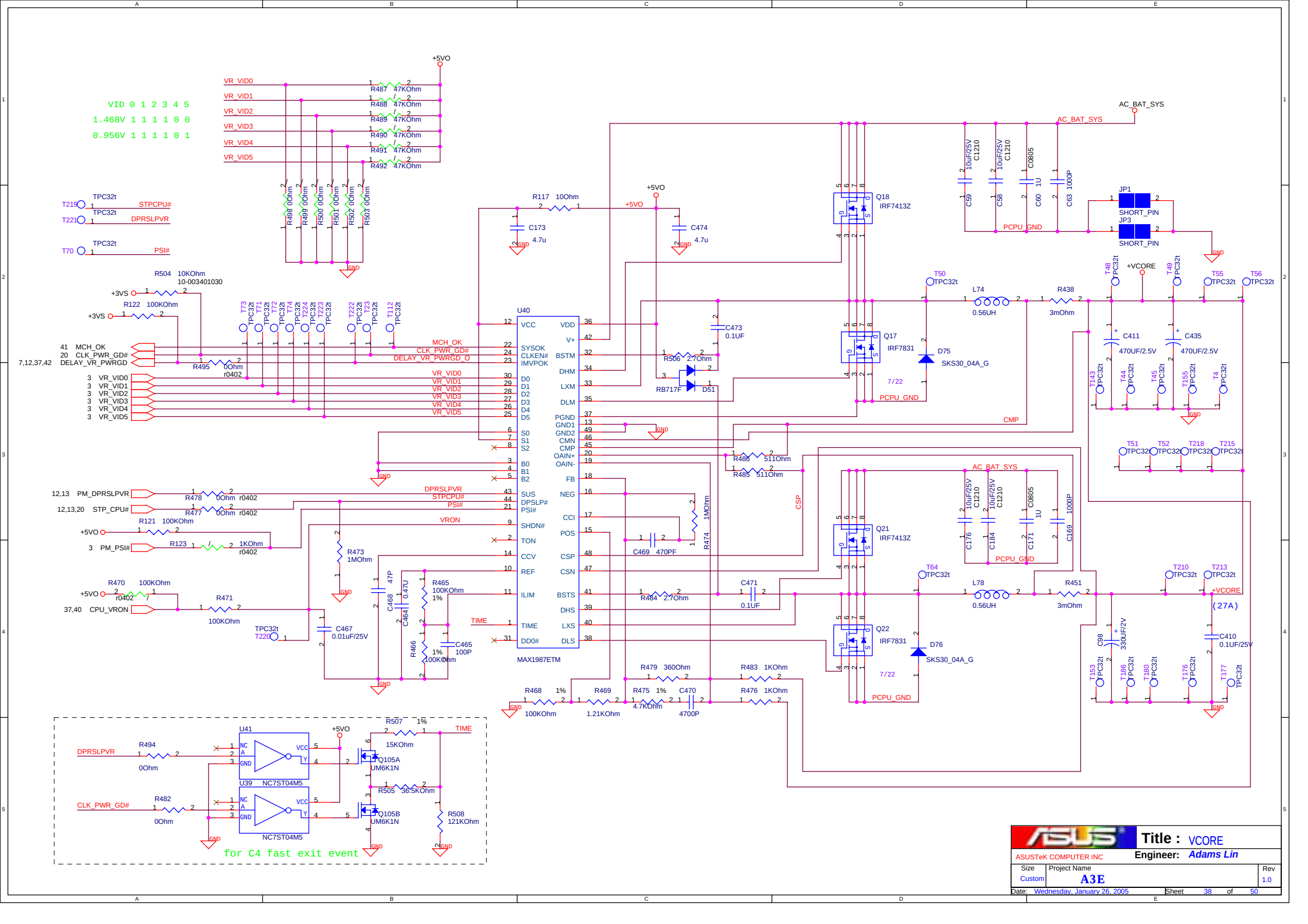
POWER ON/OFF SEQUENCE

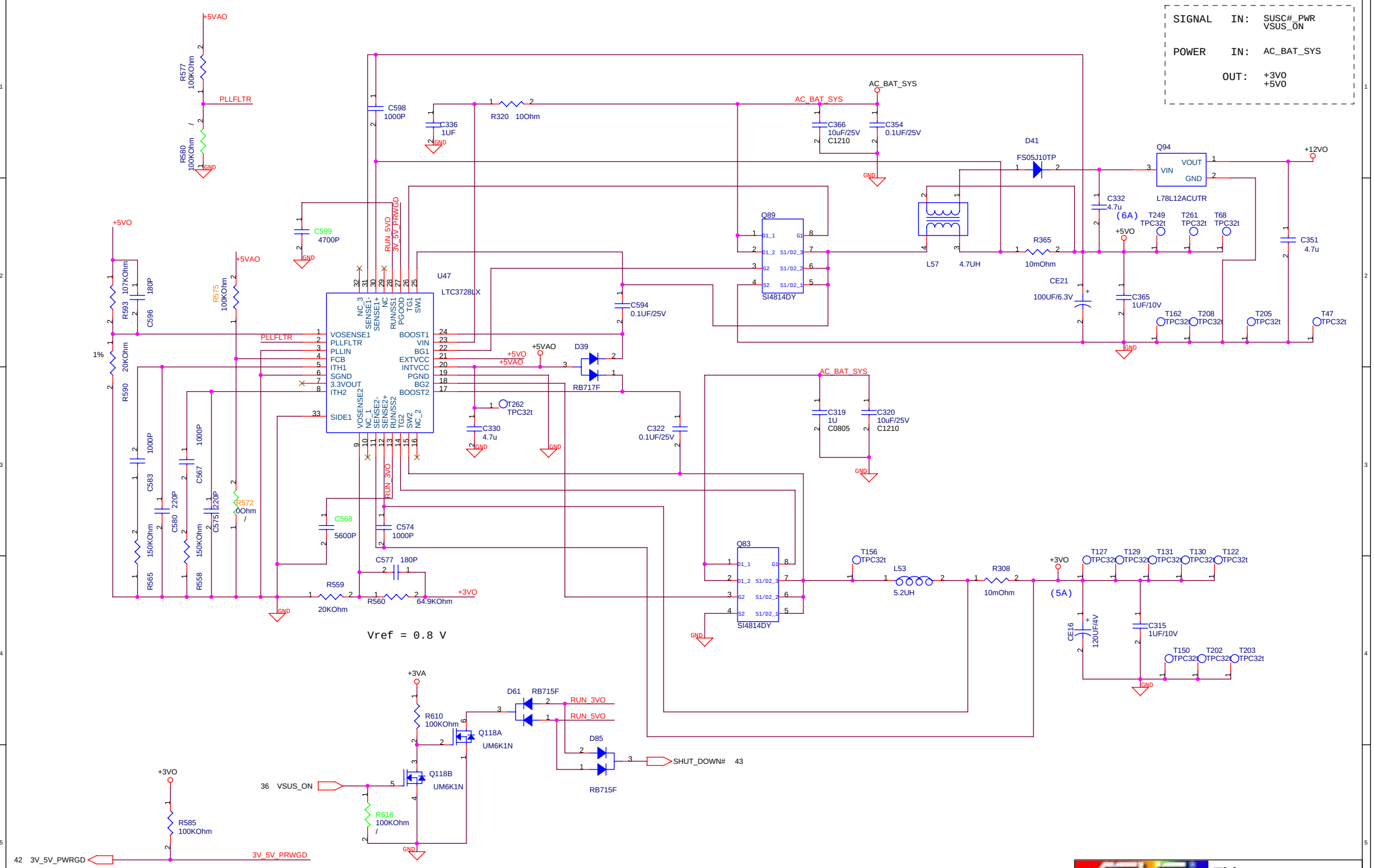
To Power circuits





ASUSTeK COMPUTER INC	Title : Startup Circuit (2)		
	Engineer: *Quan-Tai Lin*		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 37 of 50		


VID 0 1 2 3 4 5
1.468V 1 1 1 1 0 0
0.956V 1 1 1 1 0 1
U40
MAX1987ETM
U41
U39
NC7ST04M5
Q18 IRF7413Z
Q17 IRF7831
Q21 IRF7413Z
Q22 IRF7831
D75 SKS30_04A_G
D76 SKS30_04A_G
L74 0.56UH
L78 0.56UH
JP1 SHORT_PIN
JP3 SHORT_PIN
AC_BAT_SYS
PCPU_GND
+VCORE
(27A)
for C4 fast exit event
Title : VCORE
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 38 of 50


SIGNAL IN: SUSC#_PWR VSUS_ON
POWER IN: AC_BAT_SYS
OUT: +3VO +5VO
U47 LTC3728LX
Q89 SI4814DY
Q83 SI4814DY
Q94 L78L12ACUTR
D41 FS05J10TP
D39 RB717F
D61 RB715F
D85 RB715F
Q118A UM6K1N
Q118B UM6K1N
L57 4.7UH
L53 5.2UH
R320 10Ohm
R365 10mOhm
R308 10mOhm
R559 20KOhm
R560 64.9KOhm
Vref = 0.8 V
SHUT_DOWN# 43
36 VSUS_ON
42 3V_5V_PWRGD
Title : SYSTEM
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
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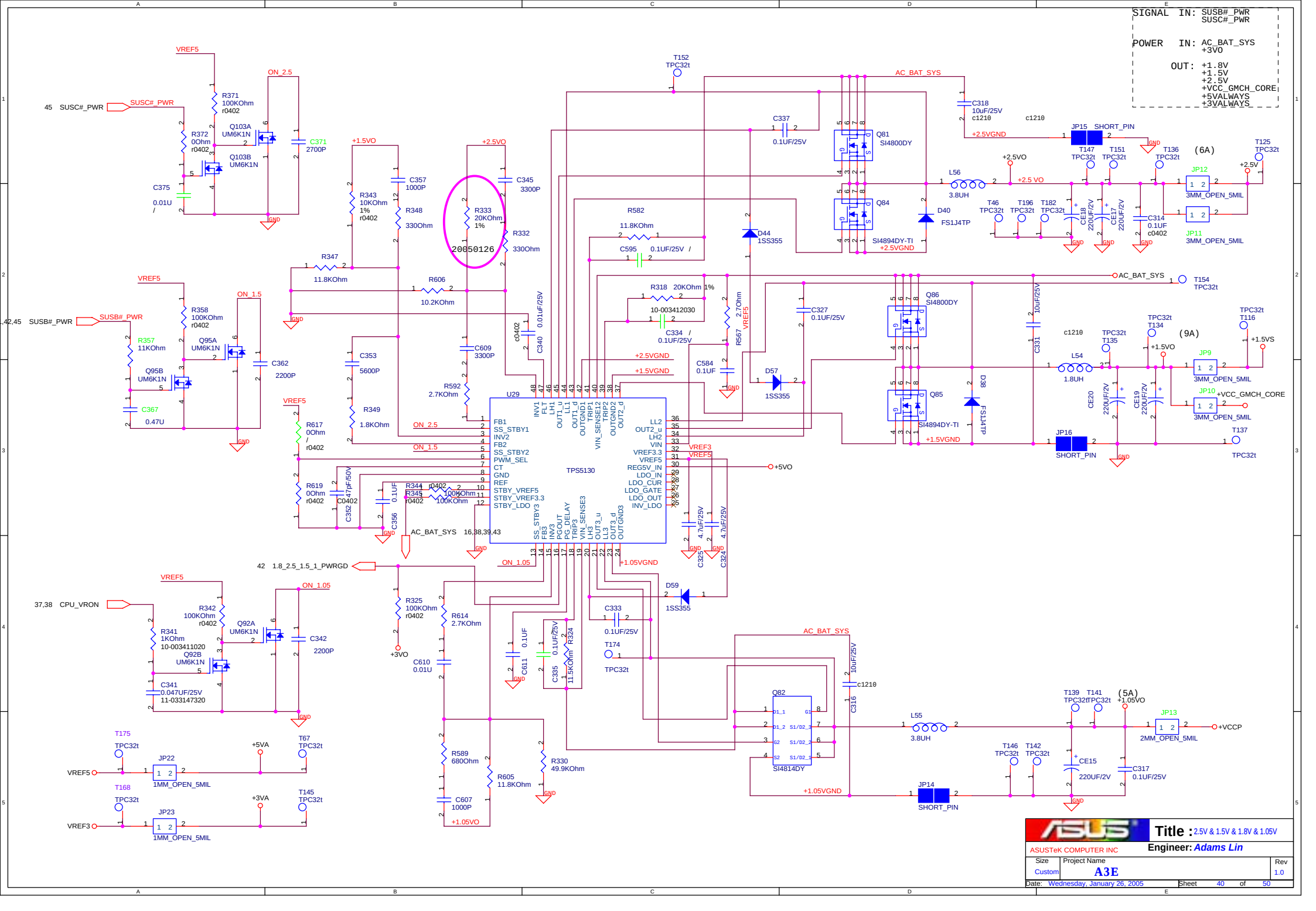
SIGNAL IN: SUSB#_PWR
SUSC#_PWR
POWER IN: AC_BAT_SYS
+3VO
OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS
TPS5130
U29
Q81 SI4800DY
Q84 SI4894DY-TI
Q86 SI4800DY
Q85 SI4894DY-TI
Q82 SI4814DY
D40 FS1J4TP
D38 FS1J4TP
D44 1SS355
D57 1SS355
D59 1SS355
L56 3.8UH
L54 1.8UH
L55 3.8UH
JP15 SHORT_PIN
JP16 SHORT_PIN
JP14 SHORT_PIN
JP12 3MM_OPEN_5MIL
JP11 3MM_OPEN_5MIL
JP9 3MM_OPEN_5MIL
JP10 3MM_OPEN_5MIL
JP13 2MM_OPEN_5MIL
JP22 1MM_OPEN_5MIL
JP23 1MM_OPEN_5MIL
(6A)
(9A)
(5A)
Title : 2.5V & 1.5V & 1.8V & 1.05V
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
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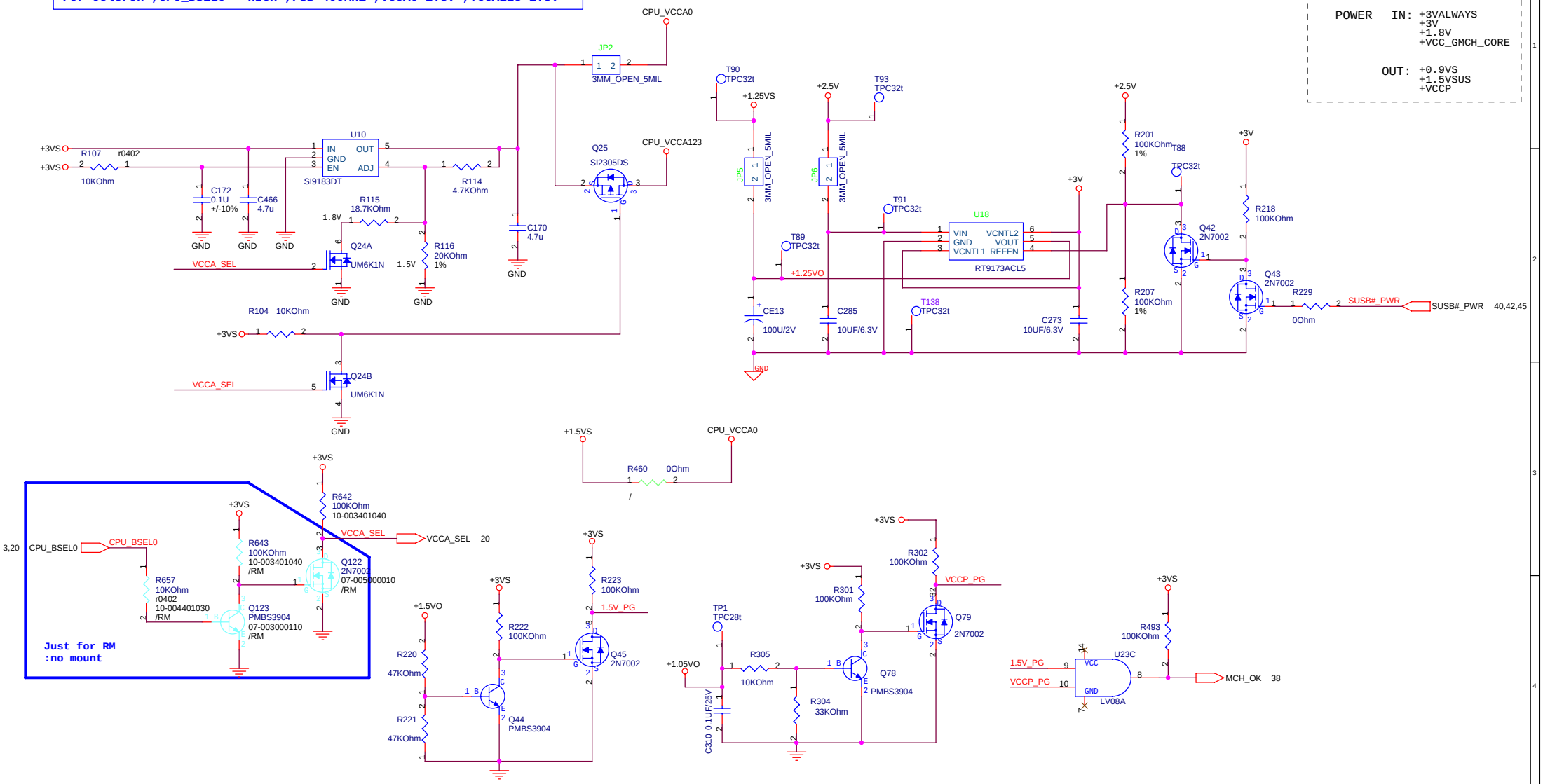
For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V

For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

SIGNAL IN: SUSB#_PWR
CPU_VRON

POWER IN: +3VALWAYS
+3V
+1.8V
+VCC_GMCH_CORE

OUT: +0.9VS
+1.5VSUS
+VCCP



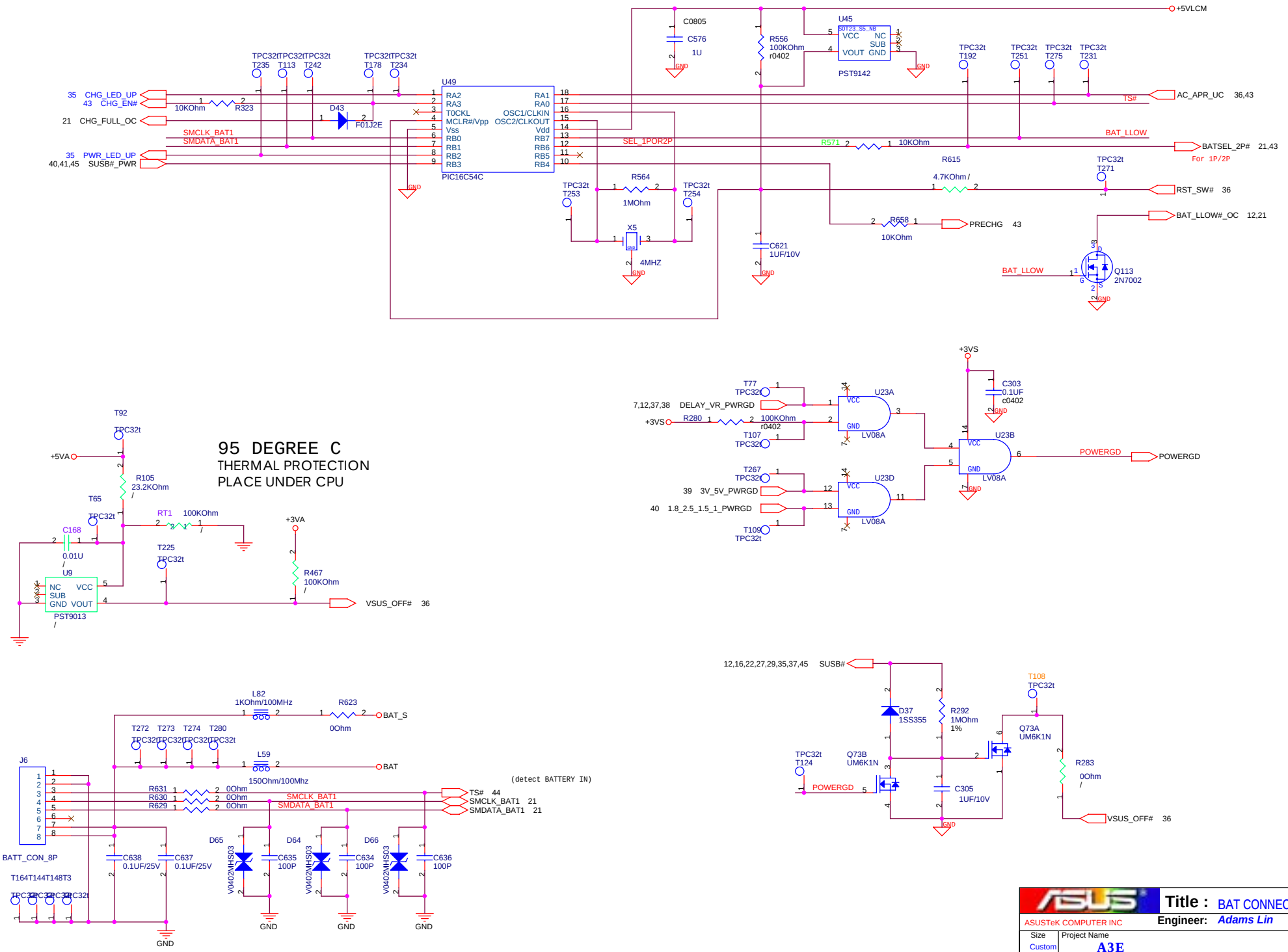
ASUSTeK COMPUTER INC

Title : 1.5VA & DDR2

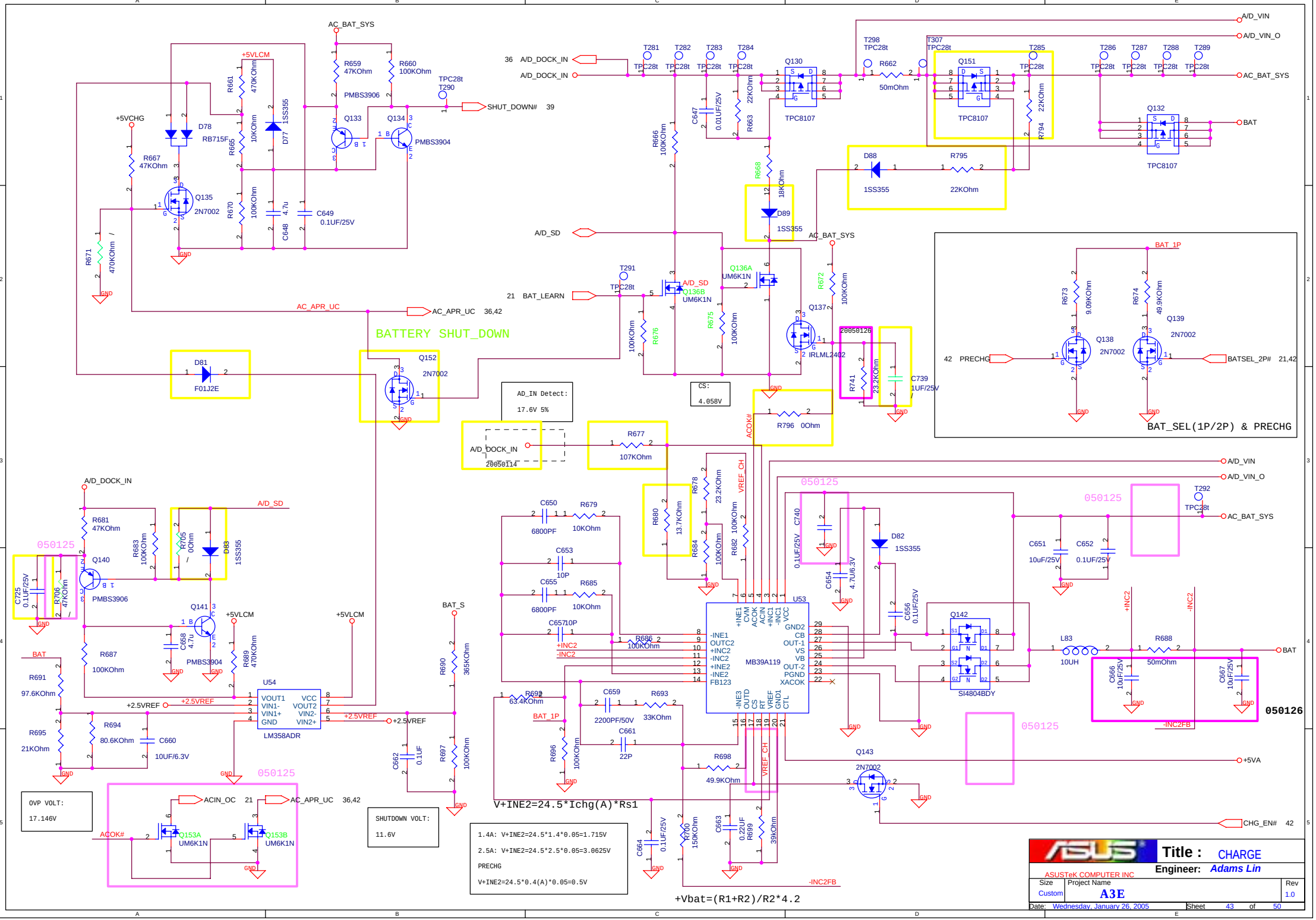
Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 41 of 50



ASUSTeK COMPUTER INC	Title : BAT CONNECT		
	Engineer: Adams Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 42 of 50		


BATTERY SHUT_DOWN
BAT_SEL(1P/2P) & PRECHG
AD_IN Detect:
17.6V 5%
CS:
4.058V
OVP VOLT:
17.146V
SHUTDOWN VOLT:
11.6V
1.4A: V+INE2=24.5*1.4*0.05=1.715V
2.5A: V+INE2=24.5*2.5*0.05=3.0625V
PRECHG
V+INE2=24.5*0.4(A)*0.05=0.5V
V+INE2=24.5*Ichg(A)*Rs1
+Vbat=(R1+R2)/R2*4.2
Title : CHARGE
Engineer: Adams Lin
ASUSTeK COMPUTER INC
Size Custom
Project Name A3E
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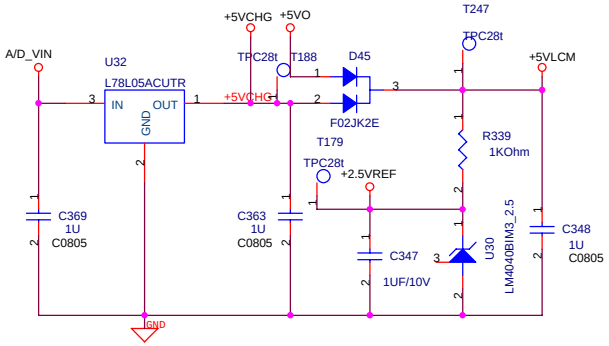
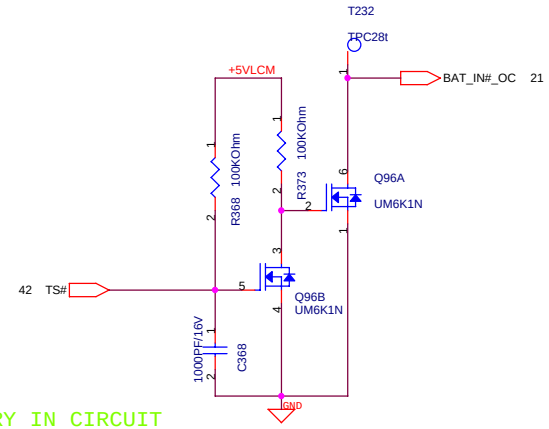
Date: Wednesday, January 26, 2005
Sheet 43 of 50

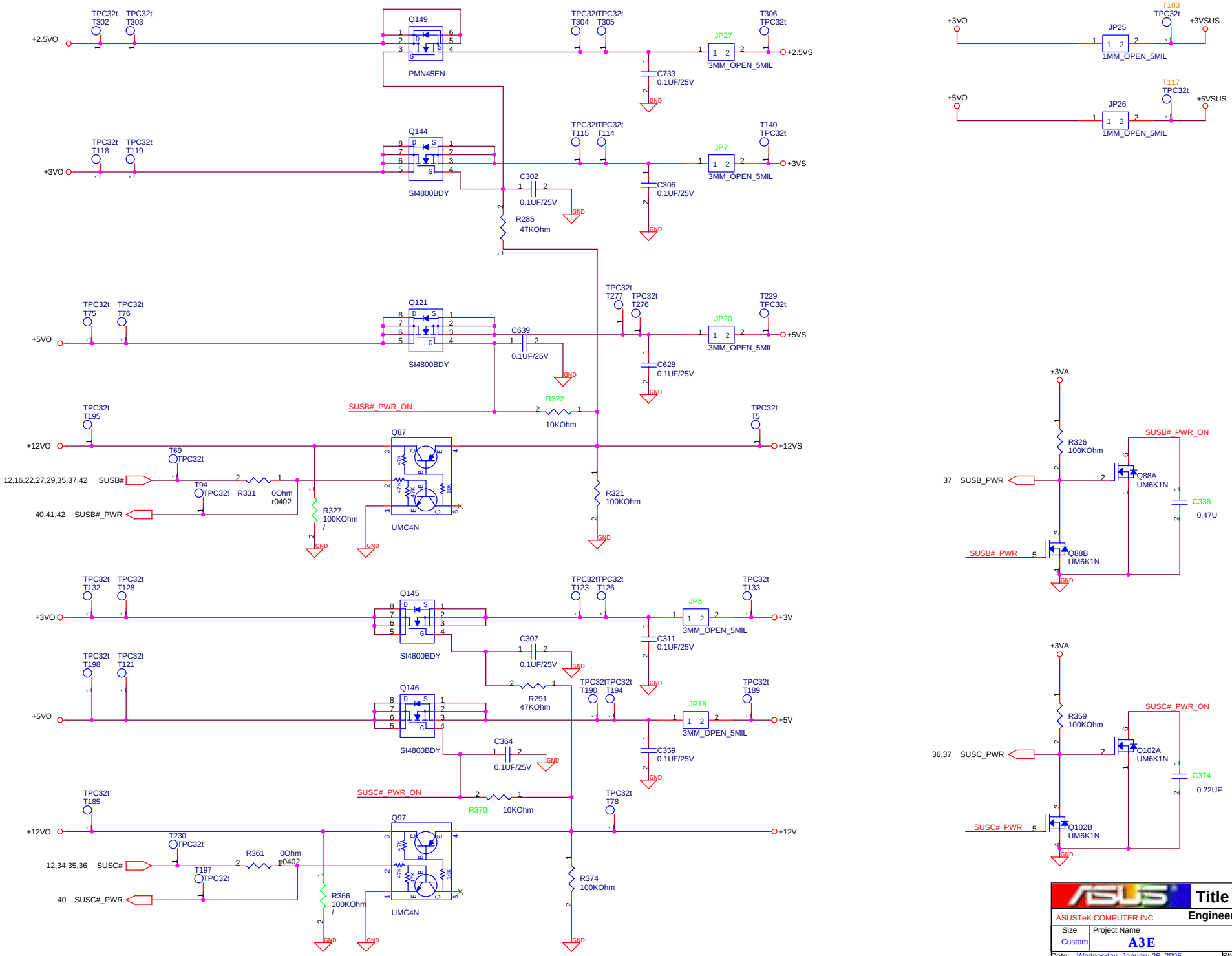


+5VCHG, +5VLCM, +2.5VREF

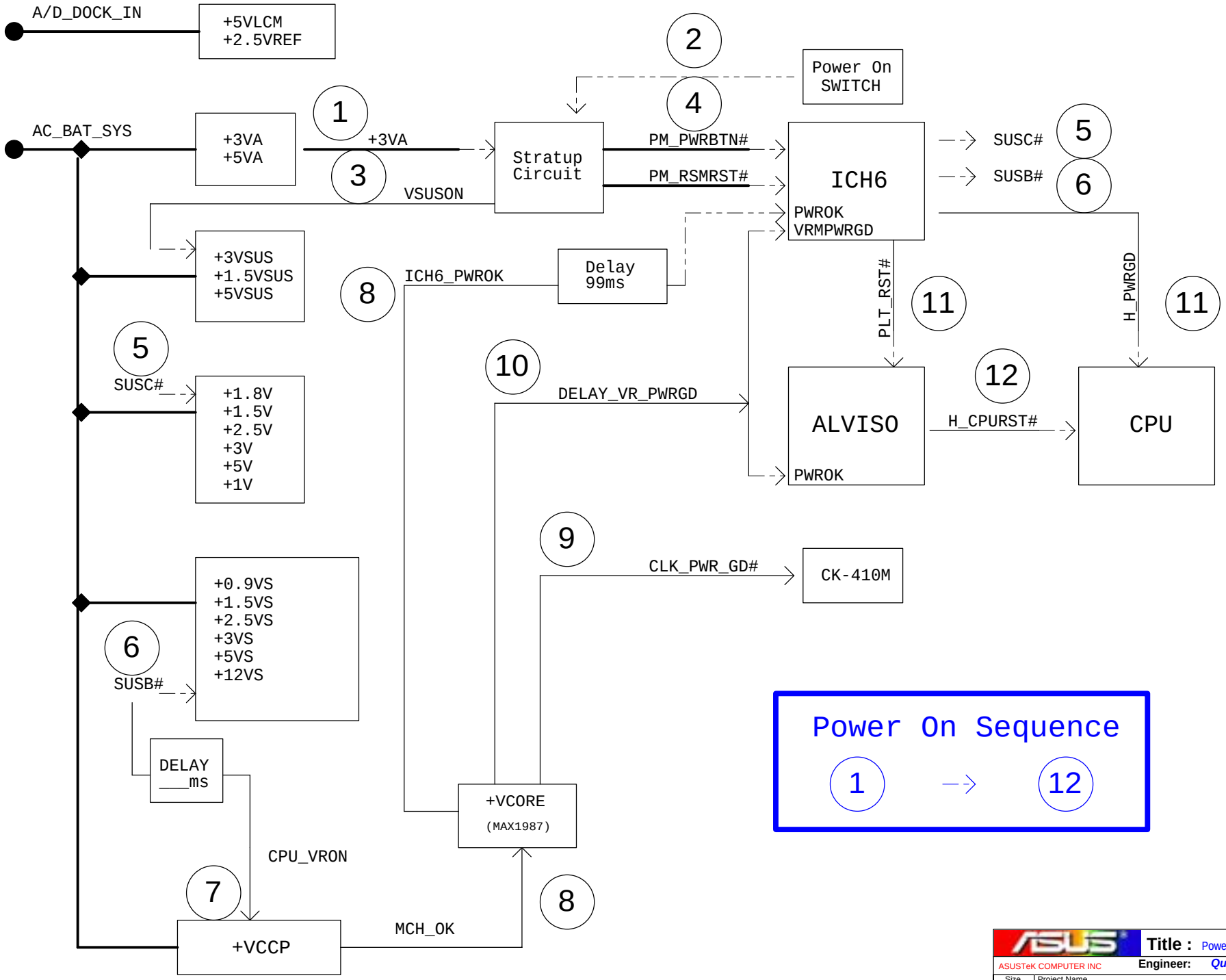


BATTERY IN CIRCUIT

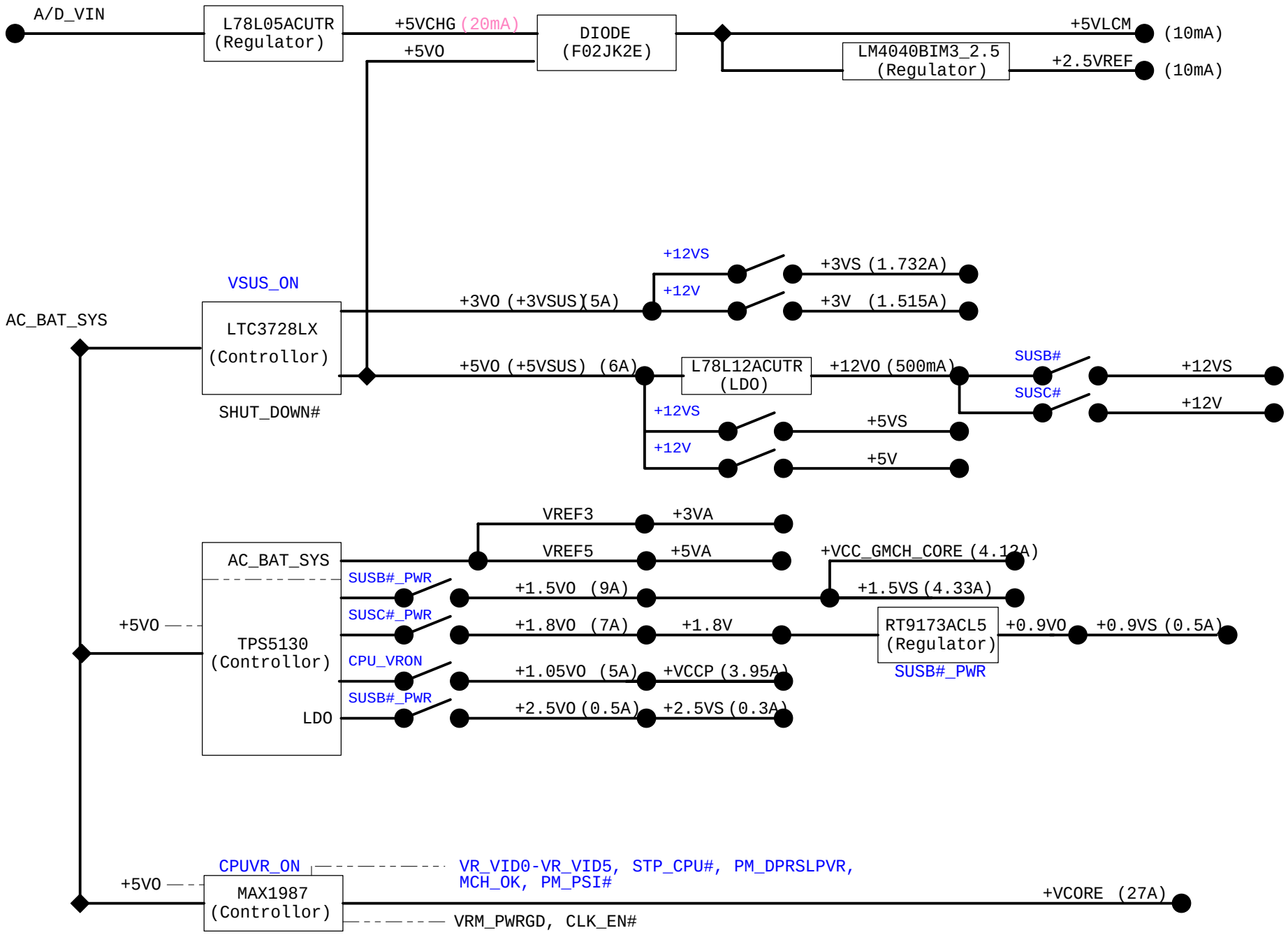
ASUS	Title : BATLOW/SD#	
ASUSTeK COMPUTER INC	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 44 of 50	



ASUSTeK COMPUTER INC	Title : LOAD SWITCH	Engineer: Adams Lin
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 45 of 50	



ASUSTeK COMPUTER INC	Title : Power On Sequence	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 46 of 50	



ASUS	Title : POWER FLOWCHART		
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 47 of 50		

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 48 of 50

Rev.	Data	Description
1.0	05' 01/06	Initial release
2005/01/21-1140		R735.R736.R750.R752 footprint change to 0603
2005/01/21-1140		JP28 for CMOS clear renames to JRST1 and no mount
2005/01/21-1140		U19.77 signal changes to ACIN_OC and R245 still mount
2005/01/21-1140		R73.R75.R76.R77 value change to 470ohm and R41 is 330ohm
2005/01/21-1140		R519 value changes to 100Kohm
2005/01/24-1035		Add SW8 ,R797 but no mount
2005/01/26-0945		R109 value changes to 820Kohm
2005/01/26-0945		D72 mount

Rev.	Data	Description
For RM:		
2005/01/24-1035		Page 31 no mount : R566,Q114,Q115,C579,C564 Page 20 no mount : R54,R43,Q16,Q19,R412 Page 41 no mount : R657,R643,Q122,Q123 Mount SW8 ,R797 Add SWITCH TABLE for CPU frequency select

ASUSTeK COMPUTER INC	Title : History-EE	
	Engineer: Quan-Tai Lin	
Size A3	Project Name A3E	Rev 1.0
Date: Wednesday, January 26, 2005	Sheet 49 of 50	

Rev.	Data	Description
1.0	05' 01/06	Initial release
	2005/01/21-1200	Add 22Kohm R794.R795 , P-MOS Q151 , diode D88.D89
	2005/01/21-1200	Add capacitor C739,resistor R796,N-MOS Q152,diode D90
	2005/01/21-1200	R677 value is from 110Kohm to 107Kohm and R677.1 connect to A/D_DOCK_IN
	2005/01/21-1200	R680 value is from 14Kohm to 13.7Kohm and D81 changes to F01J2E
	2005/01/21-1200	D83 mount and R705 no mount and R725 mount
	2005/01/26-0945	R333 value changes to 20Kohm
	2005/01/26-0945	Add Q153 for ACIN_OC and AC_APR_UC signals and delete D90
	2005/01/26-0945	Change U53.18 and U53.19 for signal VREF_CH
	2005/01/26-0945	Delete JP24 and add a cap C740 0.1UF
	2005/01/26-0945	C725 still mount and R706 no mount
	2005/01/26-0945	R741 value changes to 23.2K ohm
	2005/01/26-1250	C666 changes to connect to L83.2

Rev.	Data	Description

ASUSTeK COMPUTER INC

Title : History-PWR

Engineer: *Quan-Tai Lin*

Size	Project Name	Rev
Custom	A3E	1.0

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